SERVICE MANUAL FOR

8575

BY: Sissel Diao

TESTING TECHNOLOGY DEPARTMENT / TSSC

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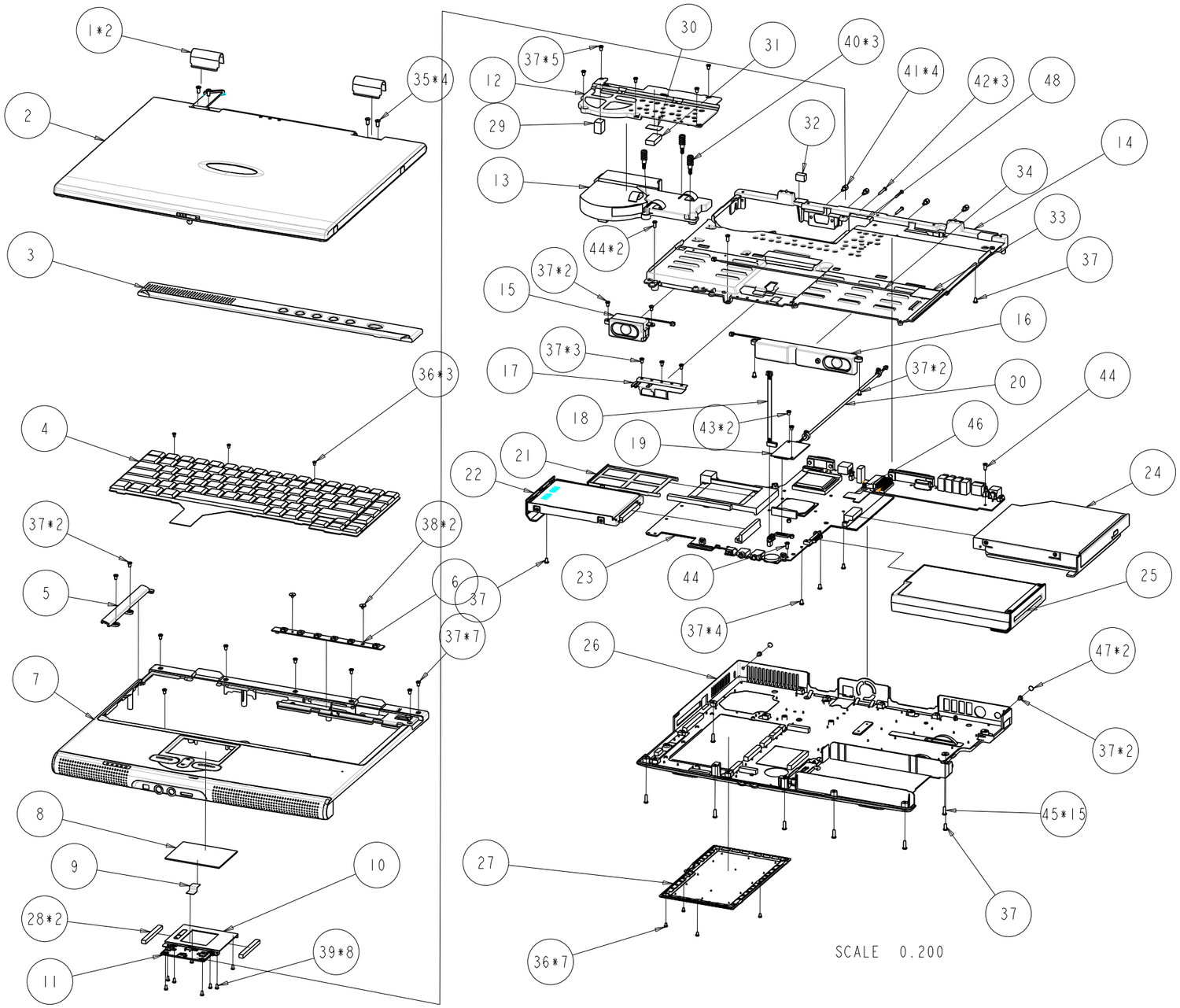
MiTAC



SCALE 0.200

ITEM	PART NO.	DESCRIPTION	Q'TY	REMARK
1	344671720023	COVER;HINGE,ID3,8575	2	
2	441671720033	LCD ASSY;QDI,XGA,14.1",ID3,8575	1	OPTION
3	340671720004	COVER ASSY;KB,ID3,8575	1	
4	531099990128	KBD OPTION;86,US,8175	1	OPTION
5	344671720002	COVER;DUMMY,ID3,8575	1	
6	411671200007	PWA;PWA-8170,ESB BD	1	
7	340671720001	COVER ASSY;ID3,8575	1	
8	442164900010	TOUCH PAD MODULE;TM41PD-350	1	
9	422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENUS	1	
10	340671600028	BRACKET ASSY;T/P,INSULATOR,8175	1	
11	411671700009	PWA;PWA-8575,T/P BD	1	
12	343671600006	PLATE;KB,8175	1	
13	340671700016	HEATSINK ASSY;P4 CPU,8575	1	
14	340671700007	SHIELDING ASSY;TOP,8575	1	
15	340671700003	SPEAKER ASSY;L,8575	1	
16	340671700008	SPEAKER ASSY;R,8575	1	
17	341671700001	SHIELDING;AUDIO,8575	1	
18	421671700001	WIRE ASSY;TOUCH PAD,8575	1	
19	412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/KIT	1	
20	421671700004	WIRE ASSY;MDC,EMI,8575	1	
21	344670500042	DUMMY CARD;PCMCIA,TETRA	1	
22	523467172006	HDD ASSY;30G,2.5",9.5MM,ID3,8575	1	OPTION
23	411671700010	PWA;PWA-8575,MOTHER BD	1	
24	523467172010	DVD ASSY;QUANTA,ID3,8575	1	OPTION
25	441999900065	BATT ASSY OPTION;LI-ION,2000mAH,8575 ID3	1	OPTION
26	340671720007	HOUSING ASSY;ID3,8575	1	
27	340671720008	COVER ASSY;DIMM,ID3,8575	1	
28	345671700009	GASKET;BRACKET T/P,8575	2	
29	345671600018	GASKET;HEATSINK,K/B_PLATE,8175	1	
30	345671700010	GASKET;KB PLATE,8575	1	
31	345671700011	GASKET;KB PLATE-1,8575	1	
32	345671600016	GASKET;LCD-HINGE,8175	1	
33	345671700019	GASKET;MIC,8575	1	
34	421671600051	MICROPHONE ASSY;8175	1	
35	370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYLOK	4	
36	370102010302	SPC-SCREW;M2L3,NIW,K-HD,736	10	
37	370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	30	
38	370102010309	SPC-SCREW;M2L3.0,NIW/NLK,HD07	2	
39	370102010407	SPC-SCREW;M2L4.K-HD,NIB/NLK	8	
40	340671200013	SCREW ASSY;CPU,8170	3	
41	377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	4	
42	371102011502	SCREW;M2L15,FLT(+),NIW/NLK	3	
43	370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	2	
44	370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	4	
45	370102610805	SPC-SCREW;M2.6L8,K-HD,NIW/NLK	15	
46	345671700002	THERMAL PAD;MOD,8575	1	
47	346671720002	INSULATOR;REAR,SCREW,ID3,8575	2	
48	340671200020	FAN ASSY;8170	1	

ITEM	CONTENTS OF CHANGE	CHK	APV	MM/DD/YY

TOL ± / RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

DATE	17-Jun-02	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.053	DRAWING NAME	LT PF;QDI,XGA,14.1",ID3,8575	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	416267172006 R00

MiTAC International Corp.

SHEET NO.2 OF 2

Model name:MAIN-ASSY-8575

File name:MAIN-ASSY-ID3-8575

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Contents

1. Hardware Engineering Specification 4

1.1 Introduction 4
1.2 System Hardware Parts 7
1.3 Other Functions 53
1.4 Peripheral Components 58
1.5 Power Management 61
1.6 Appendix 1: SiS961 GPIO Definitions 63
1.7 Appendix 2: H8 Pins Definitions 64
1.8 Appendix 3: 8575 Product Specifications 70

2. System View and Disassembly 73

2.1 System View 73
2.2 System Disassembly 76

3. Definition & Location of Connectors / Switches 94

3.1 Mother Board 94
3.2 DC Power Board 97
3.3 ESB Board 98
3.4 Touch-pad 99
3.5 Daughter Board 99

8575 N/B Maintenance

Contents

4. Definition & Location of Major Component 100

4.1 Mother Board 100

5. Pin Description of Major Component 102

5.1 Intel Pentium 4 Processor mPGA478 Socket 102

5.2 SiS650 IGUI Host / Memory Controller 108

5.3 SiS691 MuTIOL Media I/O Controller 113

5.4 SiS301LV / Chrontel CH7019 TV/LVDS Encoder 119

5.5 PCI1410GGU PCMCIA Controller 122

5.6 uPD72872 IEEE1394 Controller 127

6. System Block Diagram 129

7. Maintenance Diagnostics 130

7.1 Introduction 130

7.2 Error Codes 131

7.3 Maintenance Diagnostics 133

8. Trouble Shooting 134

8.1 No Power 135

8575 N/B Maintenance

Contents

8.2 No Display 141
8.3 VGA Controller Failure LCD No Display 145
8.4 External Monitor No Display 147
8.5 Memory Test Error 149
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error 151
8.7 Hard Disk Drive Test Error 153
8.8 CD-ROM Driver Test Error 155
8.9 USB Test Error 157
8.10 PIO Port Test Error 160
8.11 Audio Failure 162
8.12 LAN Test Error 165
8.13 PC Card Socket Failure 167
8.14 IEEE 1394 Failure 169

9. Spare Parts List 171

10. System Exploded Views 193

11. Circuit Diagram 198

12. Reference Material 230

8575 N/B Maintenance

1. Hardware Engineering Specification

1.1 Introduction

The 8575 motherboard would support the Intel® Pentium® 4 processor with FCPGA packaged, mPGA478 Socket, which will supports the different levels up to Willamette P4 1.7GHz (Throttling)/Northwood above 2.0GHz (Throttling).

This system is based on PCI architecture, which have standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 1.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 at system start up or warm reset. System also provides icon LEDs to display system status, such as power indicator, HDD/CDROM, NUM LOCK, CAP LOCK, SCROLL LOCK, SUSPEND MODE and Battery charging status. It also equipped 2 USB ports.

The memory subsystem supports 0MB on board memory, two JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM), support PC2100 & PC2700.

SiS650 IGUI Host Memory Controller integrates a high performance host interface for Intel Pentium 4 processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, an AGP 4X interface, and SiS MuTIOL® Technology connecting w/ SiS961 MuTIOL® Media I/O.

8575 N/B Maintenance

The SiS961 MuTIOL® Media I/O integrates the Audio Controller with AC 97 Interface, the Ethernet MAC, the Dual Universal Serial Bus Host Controllers, the IDE Master/Slave controllers, and the MuTIOL® Connect to PCI bridge. The PCI to LPC bridge, I/O Advanced Programmable Interrupt Controller, legacy system I/O, I/O Advanced Programmable Interrupt Controller and legacy power management functionalities are also integrated. The SiS961 also incorporates an universal interface supporting the asynchronous inputs/outputs of the X86 compatible microprocessors like PIII, K7 and P4.

The CH7019 is a Display Controller device which accepts two digital graphics input data streams. One data stream outputs through an LVDS transmitter to an LCD panel, while the other data stream is encoded for NTSC or PALTV and outputs through a 10-bit high speed DAC. The TV encoder device encodes a graphics signal up to 1024 x 768 resolution and outputs the video signals according to NTSC or PAL standards. The LVDS transmitter operates at pixel speeds up to 165MHz per link, supporting 1600 x 1200 panels at 60Hz refresh rate.

The TI PCI4410 is a dual-function PCI device compliant with *PCI Local Bus Specification 2.2*. Function 0 provides the independent PC Card socket controller compliant with the *1997 PC Card Standard*. The PCI4410 provides features that make it the best choice for bridging between the PCI bus and PC Cards, and supports either 16-bit or CardBus PC Cards in the socket, powered at 5 V or 3.3 V, as required.

Function 1 of the PCI4410 is compatible with IEEE1394A and the latest 1394 open host controller interface (OHCI) specifications. The chip provides the IEEE1394 link function and is compatible with data rates of 100, 200, and 400Mbits per second. Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies.

8575 N/B Maintenance

The PCI4410 provides physical write posting and a highly tuned physical data path for SBP-2 performance. Multiple cache line burst transfers, advanced internal arbitration, and bus holding buffers on the PHY/Link interface are other features that make the PCI4410 the best-in-class 1394 Open HCI solution.

To provide for the increasing number of multimedia applications, the AC97 CODEC ALC201 is integrated onto the motherboard.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows Me and Windows 2000 to take full advantage of the hardware capabilities such as bus mastering IDE, Windows 95-ready Plug & Play, Advanced Power Management (APM) and Advance configuration and power interface (ACPI).

Following chapters will have more detail description for each individual sub-systems and functions.

1.2 System Hardware Parts

CPU	Intel® Pentium® 4 processor; Willamette/Northwood with mFCPGA2 Package, mPGA 478 Socket Support up to Willamette P4 1.7GHz (Throttling) / Northwood above 2.0 GHz(Throttling) FSB 400MHz /PC 2100/1600
Core logic	SiS 650+SiS961: Host & Memory & AGP Controller integrates a high performance host interface for Intel Pentium 4 processor, a high performance memory controller, a AGP interface, and SiS MuTIOL® Technology connecting w/ SiS961 MuTIOL® Media IO.
VGA Control	Chrontel CH7019
System BIOS	256KB Flash EPROM Inside -Includes System BIOS, VGA BIOS, and plug & Play capability, ACPI
Memory	0MB on board memory -Two JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM) -Support PC2100 & PC2700
Video Memory	8/16/32/64 UMA
Clock Generator **DDR Clock Buffer**	ICS 952001 ICS 93722
Embedded controller	Hitachi H8 3437S
PCMCIA	Card Bus Controller: TI PCI 4410,One type II slot Card Bus TSB41AB1 of 1394 PHY
Audio System	AC97 CODEC: Advance Logic, Inc, ALC201 Power Amplifier: TI TPA0202
Super I/O	PC87393 IR Module for HP3600
Modem	56Kbps(V.90, worldwide) MDC Modem
PHY of LAN	ICS1893Y-10 10/100 base T PHY

1.2.1 CPU_Intel Pentium 4 Processor

The Intel® Pentium® 4 processor, Intel's most advanced, most powerful processor, is based on the new Intel® NetBurst™ micro-architecture. The Pentium 4 processor is designed to deliver performance across applications and usages where end users can truly appreciate and experience the performance. These applications include Internet audio and streaming video, image processing, video content creation, speech, 3D, CAD, games, multi-media, and multi-tasking user environments. The Intel Pentium 4 processor delivers this world-class performance for consumer enthusiast and business professional desktop users as well as for entry-level workstation users.

Highlights of the Pentium 4 Processor :

- Available at speeds ranging from 1.50 to 2 GHz
- Featuring the new Intel NetBurst micro-architecture
- Supported by the SiS650 chipset
- Fully compatible with existing Intel Architecture-based software
- Internet Streaming SIMD Extensions 2
- Intel® MMX™ media enhancement technology
- Memory cache ability up to 4 GB of addressable memory space and system memory scalability up to 64GB of physical memory
- Support for uni-processor designs
- Based upon Intel's 0.18 micron manufacturing process

8575 N/B Maintenance

Intel Pentium 4 Processor Product Feature Highlights

The Intel NetBurst micro-architecture delivers a number of new and innovative features including Hyper Pipelined Technology, 400 MHz System Bus, Execution Trace Cache, and Rapid Execution Engine as well as a number of enhanced features Advanced Transfer Cache, Advanced Dynamic Execution, Enhanced Floating-point and Multi-media Unit, and Streaming SIMD Extensions 2. Many of these new innovations and advances were made possible with improvements in processor technology, process technology, and circuit design that could not previously be implemented in high-volume, manufacturable solutions. The features and resulting benefits of the new micro-architecture are defined below.

- Hyper Pipelined Technology:

  The hyper-pipelined technology of the NetBurst micro-architecture doubles the pipeline depth compared to the P6 micro-architecture used on today's Pentium III processors. One of the key pipelines, the branch prediction/ recovery pipeline, is implemented in 20 stages in the NetBurst micro-architecture, compared to 10 stages in the P6 micro-architecture. This technology significantly increases the performance, frequency, and scalability of the processor.

- 400 MHZ System Bus:

  The Pentium4 processor supports Intel's highest performance desktop system bus by delivering 3.2 GB of data per second into and out of the processor. This is accomplished through a physical signaling scheme of quad pumping the data transfers over a 100-MHz clocked system bus and a buffering scheme allowing for sustained 400-MHz data transfers. This compares to 1.06 GB/s delivered on the Pentium III processor's 133-MHz system bus.

8575 N/B Maintenance

- Level 1 Execution Trace Cache:

  In addition to the 8KB data cache, the Pentium 4 processor includes an Execution Trace Cache that stores up to 12K decoded micro-ops in the order of program execution. This increases performance by removing the decoder from the main execution loop and makes more efficient usage of the cache storage space since instructions that are branched around are not stored. The result is a means to deliver a high volume of instructions to the processor's execution units and a reduction in the overall time required to recover from branches that have been mis-predicted.

- Rapid Execution Engine:

  Two Arithmetic Logic Units (ALUs) on the Pentium 4 processor are clocked at twice the core processor frequency. This allows basic integer instructions such as Add, Subtract, Logical AND, Logical OR, etc. to execute in half a clock cycle. For example, the Rapid Execution Engine on a 1.50 GHz Pentium 4 processor runs at 3 GHz.

- 256KB, Level 2 Advanced Transfer Cache:

  The Level 2 Advanced Transfer Cache (ATC) is 256KB in size and delivers a much higher data throughput channel between the Level 2 cache and the processor core. The Advanced Transfer Cache consists of a 256-bit (32-byte) interface that transfers data on each core clock. As a result, the Pentium 4 processor 1.50 GHz can deliver a data transfer rate of 48 GB/s. This compares to a transfer rate of 16 GB/s on the Pentium III processor at 1 GHz. Features of the ATC include:

  - Non-Blocking, full speed, on-die Level 2 cache
  - 8-way set associativity
  - 256-bit data bus to the level 2 cache
  - Data clocked into and out of the cache every clock cycle

8575 N/B Maintenance

- Advanced Dynamic Execution:

  The Advanced Dynamic Execution engine is a very deep, out-of-order speculative execution engine that keeps the execution units executing instructions. The Pentium 4 processor can also view 126 instructions in flight and handle up to 48 loads and 24 stores in the pipeline. It also includes an enhanced branch prediction algorithm that has the net effect of reducing the number of branch mis-predictions by about 33% over the P6 generation processor's branch prediction capability. It does this by implementing a 4KB branch target buffer that stores more detail on the history of past branches, as well as by implementing a more advanced branch prediction algorithm.

- Enhanced Floating-Point and Multimedia Unit:

  The Pentium 4 processor expands the floating-point registers to a full 128-bit and adds an additional register for data movement which improves performance on both floating-point and multimedia applications.

- Internet Streaming SIMD Extensions 2 (SSE2):

  With the introduction of SSE2, the NetBurst micro-architecture now extends the SIMD capabilities that MMX technology and SSE technology delivered by adding 144 new instructions. These instructions include 128-bit SIMD integer arithmetic and 128-bit SIMD double-precision floating-point operations. These new instructions reduce the overall number of instructions required to execute a particular program task and as a result can contribute to an overall performance increase. They accelerate a broad range of applications, including video, speech, and image, photo processing, encryption, financial, engineering and scientific applications.

- Features Used for Test and Performance / Thermal Monitoring:
  - Built-in Self Test (BIST) provides single stuck-at fault coverage of the micro-code and large logic arrays, as well as testing of the instruction cache, data cache, Translation Lookaside Buffers (TLBs), and ROMs.
  - IEEE 1149.1 Standard Test Access Port and Boundary Scan mechanism enables testing of the Pentium 4 processor and system connections through a standard interface.
  - Internal performance counters can be used for performance monitoring and event counting.
  - Includes a new Thermal Monitor feature that allows motherboards to be cost effectively designed to expected application power usages rather than theoretical maximums.

1.2.2 System Frequency

1.2.2.1 System frequency synthesizer_ICS952001

Programmable Timing Control Hub™ for P4™ processor

General Description :

The ICS952001 is a two chip clock solution for desktop designs using SIS 645/650 style chipsets. When used with a zero delay buffer such as the ICS9179-06 for PC133 or the ICS93705 for DDR applications it provides all the necessary clocks signals for such a system.

8575 N/B Maintenance

The ICS952001 is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. Employing the use of a serially programmable I2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology and a reset feature to provide a safe setting under unstable system conditions. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Recommended Application:

SiS645/650 style chipsets

Output features:

- 2 - Pairs of differential CPUCLKs @ 3.3V
- 1 - SDRAM @ 3.3V
- 8 - PCI @3.3V
- 2 - AGP @ 3.3V
- 2 - ZCLKs @ 3.3V
- 1 - 48MHz, @3.3V fixed
- 1 - 24/48MHz, @3.3V selectable by I^2C
- 3 - REF @3.3V, 14.318MHz

8575 N/B Maintenance

Features/Benefits:

- Programmable output frequency, divider ratios, output rise/fall time, output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions
- Programmable watch dog safe frequency.
- Support I^2 C Index read/write and block read/write operations
- For PC133 SDRAM system use the ICS9179-06 as the memory buffer.
- For DDR SDRAM system use the ICS93705 as the memory buffer.
- Uses external 14.318MHz crystal.

Key Specifications:

- PCI - PCI output skew: < 500ps
- CPU - SDRAM output skew: < 1ns
- AGP - AGP output skew: <150ps

1.2.2.2 DDR buffer frequency synthesizer_ICS93722

Low Cost DDR Phase Lock Loop Zero Delay Buffer

Recommended Application:

SiS645/650 style chipsets

Product description/features:

- Low skew, low jitter PLL clock driver
- I^2C for functional and output control
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- 3.3V tolerant CLK_INT input

Switching Characteristics

- PEAK - PEAK jitter (66MHz): <120ps
- PEAK - PEAK jitter (>100MHz): <75ps
- CYCLE - CYCLE jitter (66MHz): <120ps
- CYCLE - CYCLE jitter (>100MHz): <65ps
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time: 650ps - 950ps
- DUTY CYCLE: 49.5% - 50.5%

1.2.3 Core Logic_SiS650 + SiS961

1.2.3.1 SiS650 IGUI Host/Memory Controller

SiS650 IGUI Host Memory Controller integrates a high performance host interface for Intel Pentium 4 processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, an AGP 4X interface, and SiS MuTIOL® Technology connecting w/ SiS961 MuTIOL® Media IO.

SiS650 Host Interface features the AGTL & AGTL+ compliant bus driver technology with integrated on-die termination to support Intel Pentium 4 processors. SiS650 provides a 12-level In-Order-Queue to support maximum outstanding transactions up to 12. It integrated a high performance 2D/3D Graphic Engine, Video Accelerator and Advanced Hardware Acceleration MPEGI/MPEGII Video Decoder for the Intel Pentium 4 series based PC systems. It also integrates a high performance 2.1GB/s DDR266 Memory controller to sustain the bandwidth demand from the integrated GUI or external AGP master, host processor, as well as the multi I/O masters. In addition to integrated GUI, SiS650 also can support external AGP slot with AGP 1X/2X/4X capability and Fast Write Transactions. A high bandwidth and mature SiS MuTIOL® technology is incorporated to connect SiS650 and SiS961 MuTIOL® Media I/O together. SiS MuTIOL® technology is developed into three layers, the Multi-threaded I/O Link Layer delivering 1.2GB bandwidth to connect embedded DMA Master devices and external PCI masters to interface to Multi-threaded I/O Link layer, the Multi-threaded I/O Link Encoder/Decoder in SiS961 to transfer data w/ 533 MB/s bandwidth from/to Multi-threaded I/O Link layer to/from SiS650, and the Multi-threaded I/O Link Encoder/Decoder in SiS650 to transfer data w/ 533 MB/s from/to Multi-threaded I/O Link layer to/from SiS961.

8575 N/B Maintenance

An Unified Memory Controller supporting PC133 or DDR266 DRAM is incorporated, delivering a high performance data transfer to/from memory subsystem from/to the Host processor, the integrated graphic engine or external AGP master, or the I/O bus masters. The memory controller also supports the Suspend to RAM function by retaining the CKE# pins asserted in ACPI S3 state in which only AUX source deliver power. The SiS650 adopts the Shared Memory Architecture, eliminating the need and thus the cost of the frame buffer memory by organizing the frame buffer in the system memory. The frame buffer size can be allocated from 8MB to 64MB.

The Integrated GUI features a high performance 3D accelerator with 2 Pixel / 4 Texture, and a 128 bit 2D accelerator with 1T pipeline BITBLT engine. It also features a Video Accelerator and advanced hardware acceleration logic to deliver high quality DVD playback. A Dual 12 bit DDR digital video link interfaced to SiS 301B Video Bridge packaged in 100-pin PQFP is incorporated to expand the SiS650 functionality to support the secondary display, in addition to the default primary CRT display. The SiS301B Video Bridge integrates an NTSL/PAL video encoder with Macro Vision Ver. 7.1.L1 option for TV display, a TMDS transmitter with Bi-linear scaling capability for TFT LCD panel support, and an analog RGB port to support a secondary CRT. The primary CRT display and the extended secondary display (TV, TFT LCD Panel, 2'nd CRT) features the Dual View Capability in the sense that both can generate the display in independent resolutions, color depths, and frame rates.

8575 N/B Maintenance

Two separate buses, Host-t-GUI in the width of 64 bit, and GUI-t-Memory Controller in the width of 128 bit are devised to ensure concurrency of Host-t-GUI streaming, and GUI-t-MC streaming. In PC133, or DDR266 memory subsystem, the 128 bit GUI-t-MC bus will attain the AGP4X or AGP 8X equivalent texture transfer rate, respectively. The Memory Controller mainly comprises the Memory Arbiter, the M-data/M-Command Queues, and the Memory Interface. The Memory Arbiter arbitrates a plenty of memory access requests from the GUI or AGP controller, Host Controller, and I/O bus masters based on a default optimized priority list with the capability of dynamically prioritizing the I/O bus master requests in a bid to offering privileged service to 1) the isochronous downstream transfer to guarantee the min. latency & timely delivery, or 2) the PCI master upstream transfer to curb the latency within the maximum tolerant period of 10us. Prior to the memory access requests pushed into the M-data queue, any command compliant to the paging mechanism is generated and pushed into the M-CMD queue. The M-data/M-CMD Queues further orders and forwards these queuing requests to the Memory Interface in an effort to utilizing the memory bandwidth to its utmost by scheduling the command requests in the background when the data requests streamlines in the foreground.

1.2.3.2 SiS961 MuTIOL® Media I/O overview

The SiS961 MuTIOL® Media I/O integrates the Audio Controller with AC 97 Interface, the Ethernet MAC, the Dual Universal Serial Bus Host Controllers, the IDE Master/Slave controllers, and the MuTIOL® Connect to PCI bridge. The PCI to LPC bridge, I/O Advanced Programmable Interrupt Controller, legacy system I/O, I/O Advanced Programmable Interrupt Controller and legacy power management functionalities are also integrated. The SiS961 also incorporates an universal interface supporting the asynchronous inputs/outputs of the X86 compatible microprocessors like PIII, K7 and P4.

The Integrated Audio Controller features a 6 channels of AC 97 v2.2 compliance audio to present 5.1-channel Dolby digital material or to generate stereo audio with simultaneous V.90 HSP modem operation. Besides, 4 separate SDATAIN pins are provided to support multiple audio Codecs + one modem Codec maximally, effectuating the realization of 5.1 channel Dolby digital material in theater quality sound. Both traditional consumer digital audio channel as well as the AC 97 v2.2 compliant consumer digital audio slot are supported. VRA mode is also associated with both the AC 97 audio link and the traditional consumer digital audio channel.

The integrated Fast Ethernet MAC features an IEEE 802.3 and IEEE 802.3x compliant MAC supporting full duplex 10 Base-T, 100 Base-T Ethernet, or 1Mb/s & 10Mb/s Home networking. 5 wake-up Frames, Magic Packet and link status change wake-up functions in G1/G2 states are supported. Besides, the integrated MAC provides a scheme to store the MAC address without the need of an external EEPROM. The 25 MHz oscillating circuit is integrated so as only an external low cost 25 MHz crystal is needed for the clocking system.

8575 N/B Maintenance

The integrated Universal Serial Bus Host Controllers features Dual Independent OHCI Compliant Host controllers with six USB ports delivering 2 x 12 Mb/s bandwidth and rich connectivity. Besides, each port can be optionally configured as the wake-up source. Legacy USB devices as well as over current detection are also implemented. The integrated IDE Master/Slave controllers features Dual Independent IDE channels supporting PIO mode 0,1,2,3,4, and Ultra DMA 33/66/100. It provides two separate data paths for the dual IDE channels that sustain the high data transfer rate in the multitasking environment. The MuTIOL® Connect to PCI bridge supporting 6 PCI master is compliant to PCI 2.2 specification. The SiS961 also incorporates the legacy system I/O like: two 8237A compatible DMA controllers, three 8254 compatible programmable 16-bit counters, hardwired keyboard controller and PS2 mouse interface, Real Time clock with 256B CMOS SRAM and two 8259A compatible Interrupt controllers. Besides, the I/O APIC managing up to 24 interrupts with both Serial and FSB interrupt delivery modes is supported.

The integrated power management module incorporates the ACPI 1.0b compliance functions, the APM 1.2 compliance functions, and the PCI bus power management interface spec. v1.1. Numerous power-up events and power down events are also supported. 21 general purposed I/O pins are provided to give an easy to use logic for specific application. In addition, the SiS961 supports Intel Speed Step technology and Deeper Sleep power state for Intel Mobile processor. For AMD processor, the SiS961 use the CPUSTP# signal to reduce processor voltage during C3 and S1 state.

1.2.4 CH7019 TV Encoder / LVDS Transmitter

General Description

The CH7019 is a Display Controller device which accepts two digital graphics input data streams. One data stream outputs through an LVDS transmitter to an LCD panel, while the other data stream is encoded for NTSC or PALTV and outputs through a 10-bit high speed DAC. The TV encoder device encodes a graphics signal up to 1024x768 resolution and outputs the video signals according to NTSC or PAL standards. The LVDS transmitter operates at pixel speeds up to 165MHz per link, supporting 1600x1200 panels at 60Hz refresh rate.

The device can also accept one graphics data stream over two 12-bit wide variable voltage ports which support nine different data formats including RGB and YCrCb (RGB must be used for LVDS output). A maximum of 330M pixels per second can be output through dual LVDS links.

The TV-Out processor will perform non-interlaced to interlaced conversion with scaling, flicker filtering, and encoding into any of the NTSC or PAL video standards. The scaler and flicker filter are adaptive and programmable for superior text display. Eight graphics resolutions are supported up to 1024 by 768 with full vertical and horizontal under-scan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. Support is provided for MacrovisionTM. In addition to TV encoder modes, bypass modes are included which allow the TV DAC's to be used as a second CRT DAC .

8575 N/B Maintenance

The LVDS transmitter includes a panel fitting up-scaler and a programmable dither function for support of 18-bit panels. Data is encoded into commonly used formats, including those detailed in the OpenLDI and the SPWG specifications. Serialized data outputs on three to eight differential channels.

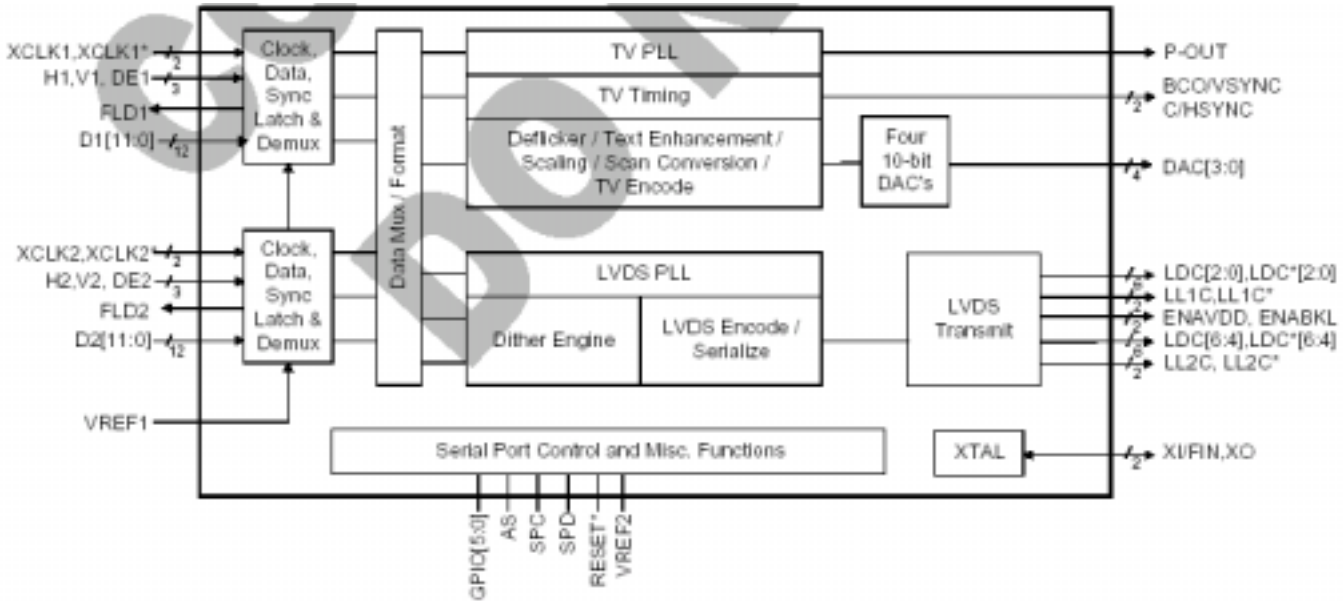


Figure 1: Functional Block Diagram

8575 N/B Maintenance

1.2.4.1 TV-Out :

- VGA to TV conversion supporting up to 1024 x 768
- MacrovisionTM 7.X copy protection support
- Two variable-voltage digital input ports
- Simultaneous LVDS and TV output
- TrueScaleTM rendering engine supports under-scan in all TV output resolutions
- Enhanced text sharpness and adaptive flicker removal with up to 7 lines of filtering
- Support for all NTSC and PAL TV formats
- Outputs CVBS, S-Video and RGB
- Support for SCART connector
- TV/Monitor connection detect
- Output video switch for easy wiring to connectors

1.2.4.2 LVDS -Out:

- Single / Dual LVDS transmitter
- Dual LVDS supports pixel rate up to 330Mpixels/sec. when both 12-bit input ports are ganged together
- Panel fitting scaler – up scale to 1600 x 1200
- VDS low jitter PLL accepts spread spectrum input
- LVDS 18-bit and 24-bit output
- 2D dither engine for 18-bit panels
- Panel protection and power down sequencing
- Programmable power management
- Hot Plug detection
- Support for second CRT DAC bypass mode
- Four 10-bit video DAC outputs
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Variable voltage interface to graphics device
- Offered in a 128-pin LQFP package

1.2.5 PC Card and OHCI Interface Controller: TI PCI4410

The PCI4410 is a dual-function PCI device compliant with *PCI Local Bus Specification 2.2*. Function 0 provides the independent PC Card socket controller compliant with the *1997 PC Card Standard*. The PCI4410 provides features that make it the best choice for bridging between the PCI bus and PC Cards, and supports either 16-bit or CardBus PC Cards in the socket, powered at 5 V or 3.3 V, as required.

All card signals are internally buffered to allow hot insertion and removal without external buffering. The PCI4410 is register compatible with the Intel™ 82365SLF and 82365SL ExCA controllers. The PCI4410 internal data path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and a pipeline architecture provide an unsurpassed performance level with sustained bursting. The PCI4410 can be programmed to accept posted writes to improve bus utilization.

Function 1 of the PCI4410 is compatible with IEEE1394A and the latest 1394 open host controller interface (OHCI) specifications. The chip provides the IEEE1394 link function and is compatible with data rates of 100, 200, and 400Mbits per second. Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The PCI4410 provides physical write posting and a highly tuned physical data path for SBP-2 performance. Multiple cache line burst transfers, advanced internal arbitration, and bus holding buffers on the PHY/Link interface are other features that make the PCI4410 the best-in-class 1394 Open HCI solution.

The PCI4410 provides an internally buffered zoomed video (ZV) path. This reduces the design effort of PC board manufacturers to add a ZV-compatible solution and ensures compliance with the CardBus loading specifications.

Various implementation-specific functions and general-purpose inputs and outputs are provided through eight multifunction terminals. These terminals present a system with options in PC/PCI DMA, PCI LOCK and parallel interrupts, PC Card activity indicator LEDs, and other platform-specific signals. ACPI-compliant general-purpose events may be programmed and controlled through the multifunction terminals, and an ACPI-compliant programming interface is included for the general-purpose inputs and outputs.

The PCI4410 is compliant with the latest *PCI Bus Power Management Specification*, and provides several low-power modes which enable the host power system to further reduce power consumption. The *PC Card (CardBus) Controller* and *IEEE 1394 Host Controller Device Class Specifications* required for Microsoft OnNow™ power management are supported. Furthermore, an advanced complementary metal-oxide semiconductor (*CMOS*) process achieves low system power consumption.

Unused PCI4410 inputs must be pulled to a valid logic level using a 43-kΩ resistor.

8575 N/B Maintenance

Features

- Ability to wake from $D3_{hot}$ and $D3_{cold}$
- Fully compatible with the Intel 430TX (Mobile Triton II) chipset
- A 208-pin low-profile QFP (PDV) or 209-ball MICROSTAR BGA™ ball grid array (GHK) package
- 3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments
- Mix-and-match 5-V/3.3-V 16-bit PC Cards and 3.3-V CardBus Cards
- Single PC Card or CardBus slot with hot insertion and removal
- Burst transfers to maximize data throughput on the PCI bus and the CardBus bus
- Parallel PCI interrupts, parallel ISA IRQ and parallel PCI interrupts, serial ISA IRQ with parallel PCI interrupts, and serial ISA IRQ and PCI interrupts
- Serial EEPROM interface for loading subsystem ID and subsystem vendor ID
- Pipelined architecture allows greater than 130M bps sustained throughput from CardBus-to-PCI and from PCI-to-CardBus
- Interface to parallel single-slot PC Card power interface switches like the TI™ TPS2211
- Up to five general-purpose I/Os
- Programmable output select for CLKRUN\
- Five PCI memory windows and two I/O windows available to the 16-bit PC Card socket
- Two I/O windows and two memory windows available to the CardBus socket

8575 N/B Maintenance

- Exchangeable Card Architecture (ExCA) compatible registers are mapped in memory and I/O space
- Intel 82365SL-DF and 82365SL register compatible
- Distributed DMA (DDMA) and PC/PCI DMA
- 16-Bit DMA on the PC Card socket
- Ring indicate, SUSPEND\, PCI CLKRUN\, and CardBus CLKRUN\
- Socket activity LED pins
- PCI bus lock (LOCK\)
- Advanced submicron, low-power CMOS technology
- Internal ring oscillator
- OHCI link function designed to *IEEE 1394 Open Host Controller Interface (OHCI) Specification*
- Implements PCI burst transfers and deep FIFOs to tolerate large host latency
- Supports physical write posting of up to 3 outstanding transactions
- OHCI link function is IEEE 1394-1995 compliant and compatible with Proposal 1394a
- Supports serial bus data rates of 100, 200, and 400Mbits/second
- Provides bus-hold buffers on the PHY-Link I/F for low-cost single-capacitor isolation

1.2.5.1 Single-Slot PC Card Power Interface Switch: TPS2211A

The TPS2211A PC Card power-interface switch provides an integrated power-management solution for a single PC Card. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit, using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V, and/or 12-V card power, and is compatible with many PCMCIA controllers. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability. Current-limit reporting can help the user isolate a system fault to the PC Card.

The TPS2211A features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5 V. Bias power can be derived from either the 3.3-V or 5-V inputs. This facilitates low-power system designs such as sleep mode and pager mode where only 3.3 V is available.

End equipment for the TPS2211A includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, and bar-code scanners.

8575 N/B Maintenance

Features

- Fully Integrated V_{CC} and V_{pp} Switching for Single-Slot PC Card™ Interface
- Low $r_{DS(on)}$ (70-m 5-V V_{CC} Switch and 3.3-V V_{CC} Switch)
- Compatible With Industry-Standard Controllers
- 3.3-V Low-Voltage Mode
- Meets PC Card Standards
- 12-V Supply Can Be Disabled Except During 12-V Flash Programming
- Short-Circuit and Thermal Protection
- Space-Saving 16-Pin SSOP (DB)
- Compatible With 3.3-V, 5-V, and 12-V PC Cards
- Break-Before-Make Switching

PC Card is a trademark of PCMCIA (Personal Computer Memory Card International Association).
LinBiCMO is a trademark of Texas Instruments. .

1.2.6 TSB41AB1, IEEE 1394a One-Port Cable Transceiver/Arbiter

The TSB41AB1 provides the digital and analog transceiver functions needed to implement a one-port node in a cable-based IEEE 1394 network. The cable port incorporates one differential line transceiver. The transceiver includes circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB41AB1 is designed to interface with a link layer controller (LLC), such as the TSB12LV21, TSB12LV22, TSB12LV23, TSB12LV26, TSB12LV31, TSB12LV41, TSB12LV42 or TSB12LV01A.

The TSB41AB1 requires only an external 24.576-MHz crystal as a reference. An external clock may be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216-MHz reference signal. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded strobe and data information. A 49.152-MHz clock signal is supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

The TSB41AB1 supports an optional isolation barrier between itself and its LLC. When the ISO\ input terminal is tied high, the LLC interface outputs behave normally. When the ISO\ terminal is tied low, internal differentiating logic is enabled, and the outputs are driven such that they can be coupled through a capacitive or transformer galvanic isolation barrier as described in Annex J of IEEE Std 1394-1995 and in IEEE 1394a-2000 (section 5.9.4) (hereinafter referred to as Annex J type isolation). To operate with TI bus holder isolation the ISO/terminal on the PHY must be high.

8575 N/B Maintenance

Data bits to be transmitted through the cable port are received from the LLC on two, four or eight parallel paths (depending on the requested transmission speed) and are latched internally in the TSB41AB1 in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304, 196.608, or 393.216Mbits/s (referred to as S100, S200, and S400 speeds, respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair, and the encoded strobe information is transmitted differentially on the TPA cable pair.

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two-, four-, or eight-bit parallel streams (depending upon the indicated receive speed), resynchronized to the local 49.152-MHz system clock and sent to the associated LLC.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage.

8575 N/B Maintenance

The TSB41AB1 provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1μF. TPBIAS is typically V_{DD} 0.2 V when the port is not connected to another node.

The line drivers in the TSB41AB1 operate in a high-impedance current mode, and are designed to work with external 112 Ω . line-termination resistor networks in order to match the 110 Ω . cable impedance. One network is provided at each end of a twisted-pair cable. Each network is composed of a pair of series-connected 56 Ω . resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair-A terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair-B terminals is coupled to ground through a parallel R-C network with recommended values of 5k Ω and 220pF. The values of the external line termination resistors are designed to meet IEEE Std 1394-1995 when connected in parallel with the internal receiver circuits. An external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents. This current-setting resistor has a value of 6.34k Ω ± 1.0%.

When the power supply of the TSB41AB1 is off while the twisted-pair cables are connected, the TSB41AB1 transmitter and receiver circuitry presents a high impedance to the cable and does not load the TPBIAS voltage at the other end of the cable. Fail-safe circuitry blocks any leakage path from the port back to the device power plane.

8575 N/B Maintenance

The TESTM, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, the TESTM terminal should be connected to V_{DD} through a 1kΩ resistor, SE should be tied to ground through a 1kΩ resistor, and SM should be connected directly to ground.

Four package terminals are used as inputs to set the default value for four configuration status bits in the self-ID packet, and are tied high through a 1kΩ resistor or hardwired low as a function of the equipment design. The PC0 C2 terminals are used to indicate the default power-class status for the node (the need for power from the cable or the ability to supply power to the cable). See Table 9 for power-class encoding. The C/LKON terminal is used as an input to indicate that the node is a contender for either isochronous resource manager (IRM) or for bus manager (BM).

The TSB41AB1 supports suspend/resume as defined in the IEEE 1394a-2000 specification. The suspend mechanism allows pairs of directly connected ports to be placed into a low-power state (suspended state) while maintaining a port-to-port connection between bus segments. While in the suspended state, a port is unable to transmit or receive data transaction packets. However, a port in the suspended state is capable of detecting connection status changes and detecting incoming TPBIAS. When the port of the TSB41AB1 is suspended, all circuits except the band gap reference generator and bias detection circuit is powered down, resulting in significant power savings. For additional details of suspend/resume operation see IEEE 1394a-2000. The use of suspend/resume is recommended for new designs.

8575 N/B Maintenance

The port transmitter and receiver circuitry is disabled during power down (when the PD input terminal is asserted high), during reset (when the RESET\ input terminal is asserted low), when no active cable is connected to the port, or when controlled by the internal arbitration logic. The TPBIAS output is disabled during power down, during reset, or when the port is disabled as commanded by the LLC.

The cable-not-active (CNA) output terminal (64-terminal PAP package only) is asserted high when there are no twisted-pair cable ports receiving incoming bias (that is, they are either disconnected or suspended), and can be used along with LPS to determine when to power down the TSB41AB1. The CNA output is not debounced. When the PD terminal is asserted high, the CNA detection circuitry is enabled (regardless of the previous state of the ports) and a pulldown is activated on the RESET\ terminal so as to force a reset of the TSB41AB1 internal logic.

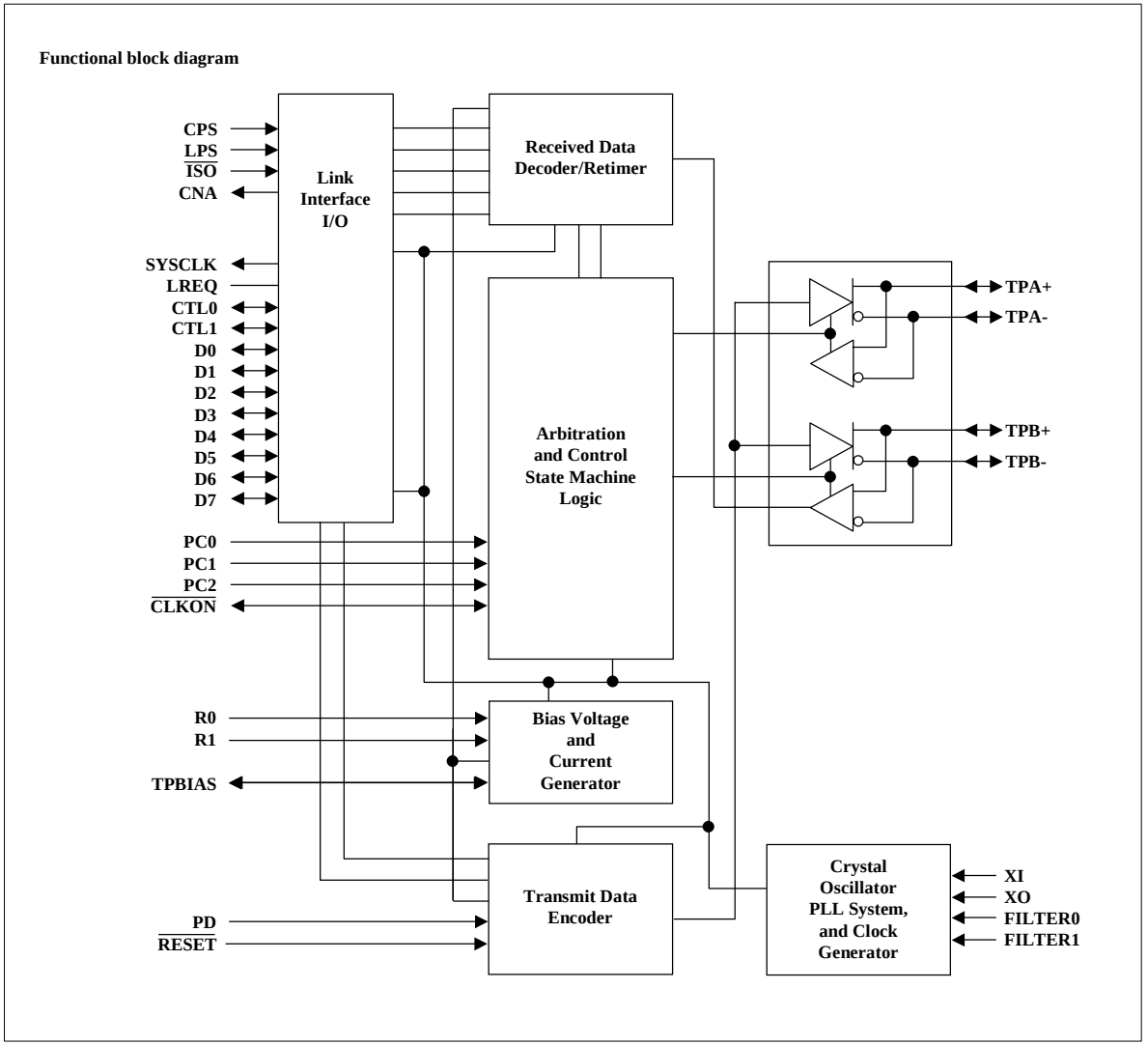
The LPS (link power status) terminal works with the C/LKON terminal to manage the power usage in the node. The LPS signal from the LLC is used in conjunction with the LCtrl bit to indicate the active/power status of the LLC. The LPS signal is also used to reset, disable, and initialize the PHY-LLC interface (the state of the PHY-LLC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit).

The LPS input is considered inactive if it remains low for more than 2.6 us and is considered active otherwise. When the TSB41AB1 detects that LPS is inactive, it places the PHY-LLC interface into a low-power reset state in which the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SYSCLK output remains active. If the LPS input remains low for more than 26 us, the PHY-LLC interface is put into a low-power disabled state in which the SYSCLK output is also held inactive. The PHY-LLC interface is also held in the disabled state during hardware reset. The TSB41AB1 continues the necessary repeater functions required for normal network operation regardless of the state of the PHY-LLC interface. When the interface is in the reset or disabled state and LPS is again observed active, the PHY initializes the interface and returns it to normal operation.

When the PHY-LLC interface is in the low-power disabled state, the TSB41AB1 automatically enters a low-power mode if the port is inactive (disconnected, disabled, or suspended). In this low-power mode, the TSB41AB1 disables its internal clock generators and also disables various voltage and current reference circuits depending on the state of the port (some reference circuitry must remain active in order to detect new cable connections, disconnections, or incoming TPBIAS, for example). The lowest power consumption (the ultralow-power sleep mode) is attained when the port is either disconnected, or disabled with the port interrupt enable bit cleared. The TSB41AB1 exits the low-power mode when the LPS input is asserted high or when a port event occurs which requires that the TSB41AB1 become active in order to respond to the event or to notify the LLC of the event (for example, incoming bias is detected on a suspended port, a disconnection is detected on a suspended port, a new connection is detected on a nondisabled port, etc.). The SYSCLK output becomes active (and the PHY-LLC interface is initialized and becomes operative) within 7.3 ms after LPS is asserted high when the TSB41AB1 is in the low-power mode.

The PHY uses the C/LKON terminal to notify the LLC to power up and become active. When activated, the C/LKON signal is a square wave of approximately 163-ns period. The PHY activates the C/LKON output when the LLC is inactive and a wake-up event occurs. The LLC is considered inactive when either the LPS input is inactive, as described above, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or when a PHY interrupt occurs. The PHY deasserts the C/LKON output when the LLC becomes active (both LPS active and the LCtrl bit set to 1). The PHY also deasserts the C/LKON output when a bus reset occurs unless a PHY interrupt condition exists which would otherwise cause C/LKON to be active.

8575 N/B Maintenance



8575 N/B Maintenance

Features

- Fully supports provisions of IEEE 1394-1995 standard for high performance serial bus and IEEE 1394a-2000
- Fully interoperable with firewire™ and i.LINK™ implementation of IEEE Std 1394
- Fully compliant with openHCI requirements
- Provides one IEEE 1394a-2000 fully compliant cable port at 100/200/400 megabits per second (Mbits/s)
- Full IEEE 1394a-2000 support includes: connection debounce, arbitrated short reset, multispeed concatenation, arbitration acceleration, fly-by concatenation, port disable/suspend/resume
- Register bits give software control of contender bit, power class bits, link active control bit, and IEEE 1394a- 2000 Features
- IEEE 1394a-2000 compliant common mode noise filter on incoming TPBIAS
- Extended resume signaling for compatibility with legacy DV devices, and terminal- and register- compatibility with TSB41LV01, allow direct isochronous transmit to legacy DV devices with any link layer even when root
- Power-Down features to conserve energy in battery powered applications include: automatic device power down during suspend, device power-down terminal, link interface disable via LPS, and inactive ports powered down
- Failsafe circuitry senses sudden loss of power to the device and disables the port to ensure that the device does not load TPBIAS of the connected device and blocks any leakage path from the port back to the device power plane
- Software device Reset (SWR)
- Industry leading low power consumption
- Ultralow-power sleep mode

- Cable power presence monitoring
- Cable ports monitor line conditions for active connection to remote node
- Data interface to link-layer controller through 2/4/8 parallel lines at 49.152MHz
- Interface to link layer controller supports low cost TI bus-holder isolation and optional annex J electrical isolation
- Interoperable with link-layer controllers using 3.3 V
- Single 3.3-V supply operation
- Low-cost 24.576MHz crystal provides transmit, receive data at 100/200/400Mbits/s, and link-layer controller clock at 49.152MHz
- Low-cost high-performance 48/64-pin TQFP (PHP/PAP) thermally enhanced packages increase thermal performance by up to 210%
- Meets Intel™ mobile power guideline 2000

1.2.7 AC'97 Audio System: Advance Logic, Inc, ALC201

SiS961 is an AC'97 2.1 compliant controller that communicates with companion Codecs SiS a digital serial link called the AC-link.

The ALC201 is an AC97 2.2 compatible stereo audio codec designed for PC multimedia systems.The ALC201 provides the way for PC98 and PC99-compliant desktop, portable and entertainment PCs, where high-quality audio is required. The ALC201 AC'97 CODEC provides a complete high quality audio solution.

8575 N/B Maintenance

Features

- Single chip audio CODEC with high S/N ratio (>90 dB)
- 18-bit ADC and DAC resolution
- Compliant with AC'97 2.2 specification
- Meet performance requirements for audio on PC2001 systems
- 18-bit stereo full-duplex CODEC with independent and variable sampling rate
- 4 analog line-level stereo input with 5-bit volume control: LINE_IN, CD, VIDEO, AUX
- 2 analog line-level mono input: PC_BEEP, PHONE_IN
- Mono output with 5-bit volume control
- Stereo output with 5-bit volume control
- 2 MIC inputs: Software selectable
- Power management
- 3D Stereo Enhancement
- Headphone output with 50mW/20ohm driving capability (ALC201)
- Line output with 50mW/20ohm driving capability (ALC201A)
- Headphone jack-detect function to mute LINE output
- Multiple CODEC extension
- MC'97 chained in allowed for multi-channel application
- External Amplifier power down capability
- Support S/PDIF out is fully compliant with AC'97 specification rev2.2

- DC offset cancellation
- Power support: Digital: 3.3V An*alog: 5V*
- Standard 48-Pin LQFP Package

1.2.8 MDC: PCTel Modem Daughter Card PCT2303W

The PCT2303W chipset is designed to meet the demand of this emerging worldwide AMR/MDC market. The combination of PC-TEL's well proven PCT2303W chipset and the HSP56TM MR software modem driver allows systems manufactures to implement modem functions in PCs at a lower bill of materials (BOM) while maintaining higher system performance.

PC-TEL has streamlined the traditional modem into the Host Signal Processing (HSP) solution. Operating with the Pentium class processors, HSP becomes part of the host computer's system software. It requires less power to operate and less physical space than standard modem solutions. PC-TEL's HSP modem is an easily integrated, cost-effective communications solution that is flexible enough to carry you into the future.

The PCT2303W chip set is an integrated direct access arrangement (DAA) and Codec that provides a programmable line interface to meet international telephone line requirements. The PCT2303W chip set is available in two 16-pin small outline packages (AC'97 interface on PCT303A and phone-line interface on PCT303W). The chip set eliminates the need for an AFE, an isolation transformer, relays, opto-isolators, and 2-to 4-wire hybrid. The PCT2303W chip set dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The PCT2303W complies with AC'97 Interface specification Rev. 2.1.

8575 N/B Maintenance

The chip set is fully programmable to meet worldwide telephone line interface requirements including those described by CTR21, NET4, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the PCT2303W chip set include AC termination, DC termination, ringer impedance, and ringer threshold. The PCT2303W chip set has been designed to meet stringent worldwide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

Operating System Compatibility

- Windows 98 /NT4.0 /Win 2K /Win XP

Compatibility

ITU-T V.90	56000, 54667, 53333,52000, 50667, 49333, 48000, 46667, 45333, 42667, 41333, 40000, 38667, 37333, 36000, 34667, 33333, 32000, 30667, 29333, 28000bps
K56Flex	56000, 54000, 52000, 50000, 48000, 46000, 44000, 42000, 40000, 38000, 36000, 32000bps
ITU-T V.34Annex	33600,31200 bps
ITU-T V.34	28800 bps
ITU-T V.32bis	14400 bps
ITU-T V.32	9600,4800 bps
ITU-T V.22bis	2400 bps
ITU-T V.22	1200 bps
ITU-T V.21	300 bps
ITU-T V.23	1200/75 bps

8575 N/B Maintenance

- ITU-T V.17 14400,12000,9600,7200 bps
- ITU-T V.29 9600,7200 bps
- ITU-T V.27ter 4800,2400 bps
- Bell 212A 1200 bps
- Bell 103 300 bps

Modulation

- 56000bps(V90&K56Flex) PCM
- 33600 bps (V.34Annex) TCM
- 28800 bps (V.34) TCM
- 14400 bps (V.32bis) TCM
- 12000 bps (V.32bis) TCM
- 9600 bps (V.32bis) TCM
- 7200 bps (V.32bis) QAM
- 9600 bps (V.32) TCM, QAM
- 4800 bps (V.32) QAM
- 14400 bps (V.17) TCM
- 12000 bps (V.17) TCM
- 9600 bps (V.29) QAM
- 7200 bps (V.29) QAM
- 4800 bps (V.27ter) DPSK

8575 N/B Maintenance

- 2400 bps (V.27ter) DPS
- 2400 bps (V.22bis) QAM
- 1200/75bps (V.23) FSK
- 1200bps(V.22/Bell 212A) DPSK
- 300bps(V.21/Bell 103) FSK

Data Compression

- V.42bis, MNP5

Error Correction

- V.42 LAPM, MNP 2-4

DTE interface

DTMF Tone Frequency

Low Group Frequency (Hz)

		697	770	852	941
High Group	1209	1	4	7	*
Frequency	1336	2	5	8	0
(Hz)	1477	3	6	9	#
	1633	A	B	C	D

DTMF signal level

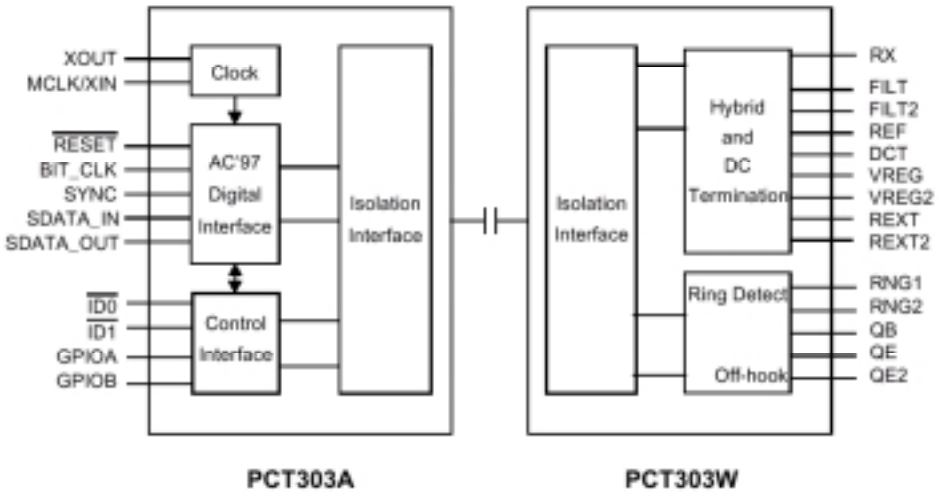
8575 N/B Maintenance

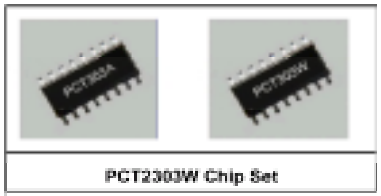
1.2.8.1 High Group -10+/-2dBm

1.2.8.2 Low Group -12+/-2dBm

- Dialing Type — Tone or pulse dialing
- Telephone Line interface — RJ-11
- Return Loss — 300HZ - 3400HZ >= 10db
- Flow Control — XOFF/XON or RTS/CTS
- Receive Level — -35 +/- 2dBm
- Transmit Level — >-15 dBm

Specification and features subject to change without notice!





8575 N/B Maintenance

1.2.9 Keyboard System: H8 (3437S) Universal Keyboard Controller

CPU	Two-way general register configuration Eight 16-bit registers or sixteen 8-bit registers High-speed operation Maximum clock rate: 16Mhz at 5V Available in temperature range: 0°C~70°C
Memory	Include 60KB ROM and 2KB RAM 16-bit free-running timer One 16-bit free-running counter Two output-compare lines Four input capture lines
8-bit timer (2 channels)	Each channel has one 8-bit up counter, two time constant registers
PWM timer (2 channels)	Resolution: 1/250 Duty cycle can be set from 0 to 100%
I^2C bus interface (one channel)	Include single master mode and slave mode
Host interface (HIF)	8-bit host interface port Three hosts interrupt requests (HIRQ1, 11,12) Regular and fast A20 gate output
Keyboard controller	Controls a matrix-scan keyboard by providing a keyboard scan function with wake-up Interrupts and sense ports
A/D converter	10-bit resolution 8 channels: single or scan mode (selectable)

8575 N/B Maintenance

- D/A converter — 8-bit resolution; 2 channels
- Interrupts — Nine external interrupt lines: NMI#, IRQ0 to 7#; 26 on-chip interrupt sources
- Power-down modes — Sleep mode; Software standby mode
- Hardware standby mode
- A single chip microcomputer
- On-chip flash memory
- Maximum 64kbyte-address space
- Support three PS/2 port for external keyboard, mouse and internal track pad.
- Support SMI, SCI trigger input:
- Cover switch
- Battery charging control
- Smart Battery monitoring
- Control D/D system on/off
- Fan control and LED indicator serial interface
- 100pin TQFP

1.2.10 System Flash Memory (BIOS)

- 2 M bit Flash memory
- Flashed by 5V only
- User can upgrade the system BIOS in the future just running flash program

1.2.11 Memory System

64MB, 128MB, 256MB, 512MB (x64) 200-Pin DDR SDRAM SODIMMs

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 200 Mb/s and 266 Mb/s DDR SDRAM components
- 64MB (8 Meg x 64 [H]); 128MB (16 Meg x 64, [H] and [HD]); 256MB (32 Meg x 64 [HD]); 512MB (64 Meg x 64 [HD])
- VDD= VDDQ= +2.5V ±0.2V
- VDDSPD = +2.2V to +5.5V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bi-directional data strobe (DQS) transmitted/received with data—i.e.,source-synchronous data capture
- Differential clock inputs (CK and CK# - can be multiple clocks, CK0/CK0#, CK1/CK1#, etc.)
- Four internal device banks for concurrent operation

- Selectable burst lengths: 2, 4 or 8
- Auto precharge option
- KBC and PS2 mouse can be individually disabled
- Auto Refresh and Self Refresh Modes
- 15.6µs (MT4VDDT864H, MT8VDDT1664HD), 7.8125µs (MT4VDDT1664H, MT8VDDT3264HD, MT8VDDT6464HD) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Serial Presence Detect (SPD) with EEPROM
- Fast data transfer rates PC2100 or PC1600
- Selectable READ CAS latency for maximum compatibility
- Gold-plated edge contacts

1.2.12 PHY: 3.3-V 10Base-T/100Base-TX Integrated PHYceiver The ICS1893 is a low-power, physical-layer device (PHY)

General Description

The ICS1893 is a low-power, physical-layer device (PHY) that supports the ISO/IEC 10Base-T and 100Base-TXCarrier-Sense Multiple Access/Collision Detection (CSMA/CD) Ethernet standards. The ICS1893 architecture is based on the ICS1892. The ICS1893 supports managed or unmanaged node, repeater, and switch applications.

8575 N/B Maintenance

The ICS1893 incorporates digital signal processing (DSP) in its Physical Medium Dependent (PMD) sublayer. As a result, it can transmit and receive data on unshielded twisted-pair (UTP) category 5 cables with attenuation in excess of 24 dB at 100 MHz. With this ICS-patented technology, the ICS1893 can virtually eliminate errors from killer packets.

The ICS1893 provides a Serial Management Interface for exchanging command and status information with a Station Management (STA) entity.

The ICS1893 Media Dependent Interface (MDI) can be configured to provide either half- or full-duplex operation at data rates of 10 MHz or 100 MHz. The MDI configuration can be established manually (with input pins or control register settings) or automatically (using the Auto-Negotiation features). When the ICS1893 Auto-Negotiation sublayer is enabled, it exchanges technology capability data with its remote link partner and automatically selects the highest-performance operating mode they have in common.

Features

- Supports category 5 cables with attenuation in excess of 24 dB at 100 MHz across a temperature range from -5 to +85 C
- DSP-based baseline wander correction to virtually eliminate killer packets across temperature range from -5 to +85 C
- Low-power, 0.35-micron CMOS (typically 400 mW)
- Single 3.3-V power supply

8575 N/B Maintenance

- Single-chip, fully integrated PHY provides PCS, PMA, PMD and AUTONEG sublayers of IEEE standard
- 10Base-T and 100Base-TX IEEE 802.3 compliant
- Fully integrated, DSP-based PMD includes:
  - Adaptive equalization and baseline wander correction
  - Transmit wave shaping and stream cipher scrambler
  - MLT-3 encoder and NRZ/NRZI encoder
- Highly configurable design supports:
  - Node, repeater, and switch applications
  - Managed and unmanaged applications
  - 10M or 100M half- and full-duplex modes
  - Parallel detection
  - Auto-negotiation, with Next Page capabilities
- MAC/Repeater Interface can be configured as:
  - 10M or 100M Media Independent Interface
  - 100M Symbol Interface (bypasses the PCS)
  - 10M 7-wire Serial Interface
- Small Footprint 64-pin Thin Quad Flat Pack (TQFP)

1.3 Other Functions

1.3.1 Hot Key Functions

Keys Combination	Feature	Meaning
Fn + F1	Reserve	
Fn + F2	Reserve	
Fn + F3	Volume Down	
Fn + F4	Volume Up	
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only, and simultaneously display.
Fn + F6	Brightness down	Decreases the LCD brightness
Fn + F7	Brightness up	Increases the LCD brightness
Fn + F8	Brightness MAX	Toggle Max Brightness
Fn + F9	Pause	
Fn + F10	Break	
Fn + F11	Panel Off/On	Toggle Panel on/off
Fn + F12	Suspend to DRAM / HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup.

1.3.2 Power on/off/suspend/resume button

APM mode

At APM mode, Power button is on/off system power.

APM mode

At ACPI mode. Windows power management control panel set power button behavior.
You could set “standby”, “power off” or “hibernate”(must enable hibernate function in power Management) to power button function.
Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.
At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby
3. Off
4. Hibernate (must enable hibernate function in power management)

1.3.4 Reset Switch

There is a reset switch at bottom side of notebook. It will reset embedded controller H8 and turn off system totally. When system hands up and Power button has no function, this switch is the only way to turn off system without remove power source.

1.3.5 LED Indicators

System has eight status LED indicators to display system activity, which include three at front side and five above keyboard.

1) Three LED indicators at front side:

From left to right that indicates: AC Power, Battery Power and Battery Status

- AC Power: This LED lights green when AC is powering the notebook, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries.
- Battery Power: This LED lights green when the notebook is being powered by Battery, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using Battery power. The LED is off when the notebook is off or powered by batteries, or when Suspend to Disk.
- Battery Status: During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged.

2) Five LED indicators above keyboard:

From left to right that indicates LAN, CD-ROM/HARD DISK DRIVE, NUM LOCK, CAPS LOCK and SCROLL LOCK.

1.3.6 Battery Status

Battery Warning

System also provides Battery capacity monitoring and gives user a warning so that users have chance to save his data before battery dead. Also, this function protects system from mal-function while battery capacity is low.

Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds. System will suspend to HDD after 2 Minutes to protect users data.

Battery Low State

After Battery Warning State, and battery capacity is below 4%, system will generate beep for twice per second.

Battery Dead State

When the battery voltage level reaches 7.4 volts, system will shut down automatically in order to extend the battery packs' life.

1.3.7 Fan power on/off management

FAN is controlled by H8 embedded controller-using AD2201 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.3.8 CMOS Battery

- CR2032 3V 220mAh lithium battery
- When AC in or system main battery inside, CMOS battery will consume no power.
- AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years.
- Battery was put in battery holder, can be replaced.

1.3.9 I/O Port

- One Power Supply Jack.
- One External CRT Connector For CRT Display
- Supports two USB port for all USB devices.
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN.
- Headphone Out Jack.
- Microphone Input Jack.
- Line in Jack
- One Card Bus Sockets for one type II PC card extension

1.3.10 Battery current limit and learning

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.4 Peripheral Components

1.4.1 LCD Panel

- LCD 14.1 Hyundai HT14X12-100A

1.4.2 Ext.Floppy Disk Drive

- Mitsumi D353GU
- External USB 3.5” 1.44MB /1.2 MB/720KB FDD (Option)

1.4.3 HDD

- Hitachi 30GB
- Height: 9.5 mm, 2.5”

1.4.4 24X CD-ROM Drive

- TEAC

1.4.5 8W/4R CD-RW

- KEM
- Height: 12.7 mm IDE I/F

1.4.6 Keyboard

Windows 98 Keyboard, 1 color, multi languages support JP, US and Europe Keyboard with “ Volume UP ” and “ Volume Down ” word.

1.4.7 Track Pad Synaptics

- Accurate positioning
- Low fatigue pointing action
- Low profile
- No moving part, high reliability
- Low power consumption
- Environmentally sealed
- Compact size.
- Software configurable
- Low weight
- Operating temperature: 0 to 60 degree C

1.4.7 Track Pad Synaptics

- Operating humidity: 5%-95% relative humidity, non condensing
- Storage temperature: -40 to +65 degree C
- ESD: 15KV applied to front surface SEE ESD Testing specification PN 520-000270-01
- Power supply voltage: 5.0Voltage ± 10%
- Power supply current: 4.0mA max operating

1.4.8 Fan

- HY45J05-001

1.4.9 Memory

- DDR-RAM/ATP//128M/256M
- DDR-RAM/Apacer//128M/256M
- DDR-RAM/Unidorsa//128M/256M

1.4.10 Modem MDC

- Askey

1.5 Power Management

The 8575 system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.5.1 System Management Mode

Full on mode

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability. The CPU power consumption and temperature is lower in this mode.

Standby mode

For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

- CPU: Stop grant
- LCD: backlight off
- HDD: spin down

Suspend to DRAM

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

- Suspend to DRAM:
  - CPU: off
  - Twister K: Partial off
  - VGA: Suspend
  - PCMCIA: Suspend
  - Audio: off
  - SDRAM: self refresh
- Suspend to HDD:
  - All devices are stopped clock and power-down
  - System status is saved in HDD
  - All system status will be restored when powered on again

1.5.2 Other Power Management Functions

HDD & Video access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.6 Appendix 1: SiS961 GPIO Definitions

SB_SiS961 GPIO

Signal Name	MUX Function	Mitac Definition	Buffer Type	Power Plane	Tolerant	During PCISRT#	After PCISRT#	S1	S3	S4/S5
GPIO0		MB_ID0	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO1	LDRQ1#	CD_IN#	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO2	THERM#	SB_THRM#	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO3	EXTSMI#	EXTSMI#	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO4	CLKRUN#	CLKRUN#	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO5	PREQ5#	LCD_ID0	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO6	PGNT5#	LCD_ID1	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO7		LCD_ID2	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO8	RING#	WAKEUP#	I/O	AUX		High-Z	High-Z	High-Z	High-Z	High-Z
GPIO9	AC_SDIN2	SCI#	I/O	AUX		High-Z	High-Z	High-Z	High-Z	High-Z
GPIO10	AC_SDIN3	CRT_IN#	I/O	AUX		High-Z	High-Z	High-Z	High-Z	High-Z
GPIO11		SPK_OFF	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO12	CPUSTP#	CPU_STP#	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO13	DPRSLPVR	MPCIACT# /DPRSLPVR	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO14		CD_PWRON#	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO15	VR_HILO#	VR_HILO#	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO16	LO_HI#	LO_HI#	OD	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO17	VGATEM#	VGATEM#	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO18	PMCLK	CD_RST	O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO19	SMBCLK	SMBCLK	O	AUX		High-Z	High-Z	High-Z	High-Z	High-Z
GPIO20	SMBDATA	SMBDATA	O	AUX		High-Z	High-Z	High-Z	High-Z	High-Z

1.7 Appendix 2: H8 Pins Definitions

The shadowed block is the selected function

Name	Pin	H8 Pin Definitions	During RESET	After RESET/OFF		ON		STANDBY		Function
MD0	6	H8_MODE0	I ↑	I	H	I	H	I	H	H H mode3 single chip mode
MD1	5	H8_MODE1	I ↑	I	H	I	H	I	H	
STBY#	8	STBY#	I ↑	I	H	I	H	I	H	H8 Hardware Standby input pull high
NMI#	7	POWER BTN#	I ↑	I	H	I	HL H	I	H	Power button
RESET#	1	RESET#	I	I	LH	I	H	I	H	H8 chip reset
XTAL	2	Crystal	I	I		I		I		Crystal input
EXTAL	3	Crystal	I	I		I		I		
RESET OUT#	100	RESET OUT	O	O		O		O		
Port A COMOS input level (input high min=3.5V, input low max=1.0V)										
PA0	48	LID#	I ↑	I	H	I		I	H	
PA1	47	H8 ADEN#	I ↑	I	H/L	I		I	H/L	AC adaptor in detect
PA2	31	RI#	I ↑	I	H	I		I	H	Ring detect
PA3	30	BATT DEAD#	I ↑	I	H	I		I	H	Battery low detect
PA4	21	H8 SUSC	I ↑	I	H	I		I	L	System resume from S4 soft off through RTC Alarm
PA5	20	H8 SUSC#	I ↑	I	L	I		I	H	System to S4 soft off
PA6	11	BAT_CLK	I ↑	I	L	I		I	H	
PA7	10	H8_SUSB	I ↑	I	H	I	L	I	H	Invert from SUSA# to wake up H8 when system resumed by MDC modem and internal LAN. Inform system power management status

8575 N/B Maintenance

PCI reset gate

Name	Pin	H8 Pin Definitions	During RESET	After RESET/OFF	ON		STANDBY		Function
Port B TTL input voltage (input high min=2V, input low max=0.8V)									
PB0	91	H8 SB PWRBTN#	T	O	L	IHL	O	Keep H	Power button trigger VIA8231 on/off Duplicate Power BTN# 5→3V
PB1	10	H8 WAKE#	T	O	H	O	O	Keep H	Wake up SB at ACPI mode 5→3V
PB2	81	Force Discharge	T	O			O	Keep H	Power button trigger VIA8231 on 5→3V
PB3	80	CHARGING1	T	O	LLH	O	O	Keep	Battery charge control
PB4	69	VDD5 SW	T↓	O	L	O H	O	Keep H	H8 VDD5 power source switch
PB5	68	H8 RCIN#	T	O		O LH	O	Keep H	Reset CPU
PB6	58	CHARGING2	T	O		O	O	Keep	Battery charge control
PB7	57	SMbus SW	T	O		O	O	Keep	
PB6	58	VADJ1	T	O		O	O	Keep	Lithium ion battery charging CV mode voltage level adjust
PB7	57	VADJ2	T	O		O	O	Keep	
Port 1 TTL input voltage (input high min=2V, input low max=0.8V)									
P10/A0	79	KB OUT0	L	O	L	O LH	O	Keep L	Key matrix scan output 0
P11/A1	78	KB OUT1	L	O	L	O LH	O	Keep L	Key matrix scan output 1
P12/A2	77	KB OUT2	L	O	L	O LH	O	Keep L	Key matrix scan output 2
P13/A3	76	KB OUT3	L	O	L	O LH	O	Keep L	Key matrix scan output 3
P14/A4	75	KB OUT4	L	O	L	O LH	O	Keep L	Key matrix scan output 4
P15/A5	74	KB OUT5	L	O	L	O LH	O	Keep L	Key matrix scan output 5
P16/A6	73	KB OUT6	L	O	L	O LH	O	Keep L	Key matrix scan output 6
P17/A7	72	KB OUT7	L	O	L	O LH	O	Keep L	Key matrix scan output 7

Continue to previous

Name	Pin	H8 Pin Definitions	During RESET	After RESET/OFF		ON		STANDBY		Function
Port 2 TTL input voltage (input high min=2V, input low max=0.8V)										
P20/A8	67	KB OUT8	L	O	L	O	LH	O	Keep L	Key matrix scan output 8
P21/A9	66	KB OUT9	L	O	L	O	LH	O	Keep L	Key matrix scan output 9
P22/A10	65	KB OUT10	L	O	L	O	LH	O	Keep L	Key matrix scan output 10
P23/A11	64	KB OUT11	L	O	0	O	LH	O	Keep L	Key matrix scan output 11
P24/A12	63	KB OUT12	L	O	0	O	LH	O	Keep L	Key matrix scan output 12
P25/A13	62	KB OUT13	L	O	0	O	LH	O	Keep L	Key matrix scan output 13
P26/A14	61	KB OUT14	L	O	0	O	LH	O	Keep L	Key matrix scan output 14
P27/A15	60	KB OUT15	L	O	0	O	LH	O	Keep L	Key matrix scan output 15
Port 3 TTL input voltage (input high min=2V, input low max=0.8V)										
P30/HDB0/D0	82	ISA SD0	T	I/O		I/O		I/O	Keep	ISA DATA bit 0
P31/HDB1/D1	83	ISA SD1	T	I/O		I/O		I/O	Keep	ISA DATA bit 1
P32/HDB2/D2	84	ISA SD2	T	I/O		I/O		I/O	Keep	ISA DATA bit 2
P33/HDB3/D3	85	ISA SD3	T	I/O		I/O		I/O	Keep	ISA DATA bit 3
P34/HDB4/D4	86	ISA SD4	T	I/O		I/O		I/O	Keep	ISA DATA bit 4
P35/HDB5/D5	87	ISA SD5	T	I/O		I/O		I/O	Keep	ISA DATA bit 5
P36/HDB6/D6	88	ISA SD6	T	I/O		I/O		I/O	Keep	ISA DATA bit 6
P37/HDB7/D7	89	ISA SD7	T	I/O		I/O		I/O	Keep	ISA DATA bit 7

8575 N/B Maintenance

Continue to previous

Name	Pin	H8 Pin Definitions	During RESET	After RESET/OFF		ON		STANDBY		Function
Port 4 TTL input voltage (input high min=2V, input low max=0.8V)										
P40/TMCI0	49	H8 PWR ON	T↓	O	L	O	LH	O	Keep	System power on, need pull down to define initial state during reset
P41/TMO0	50	H8 THRM#	T	O	L	O	H	O	Keep H	Thermal throttling control to Southbridge
P42/TMRI0	51	SCI#/ FAN SPD SW	T	O	H			O	Keep	SCI output and Fan Speed Tachometer Switch
P43/TMCI1/HIRQ1	52	H8 SCI/ FAN SPEED	T	O		O		O	Keep	Need invert to SCI# sending to SB 5→3V/ Fan speed tachometer
P44/TMCO1/HIRQ1	53	ISA IRQ1	T	O	0	O		O	Keep	Keyboard IRQ1
P45/TMRI1/HIRQ1	54	ISA IRQ12	T	O	0	O		O	Keep	PS2 mouse IRQ12
P46/PWM0	55	Beep sound	T	O		O		O	Keep	Hot key and battery dead beep sound
P46/PWM0	55	FAN ON#0	T	O	1	O		O	Keep	Fan power PWM control
P47/PWM1	56	FAN ON#1	T	O	1	O		O	Keep	Fan power PWM control
Port 5 TTL input voltage (input high min=2V, input low max=0.8V)										
P50/TXD0	14	LED DATA	T	O		O		O	Keep	LED indicator shift data
P51/RXD0	13	H8 SMI#	T	O		O		O	Keep	External SMI# 5→3V
P52/SCK0	12	LED CLK	T	O		O		O	Keep	LED indicator shift clock

Continue to previous

Name	Pin	H8 Pin Definitions	During RESET	After RESET/OFF		ON	STANDBY		Function
Port 6 Schmitt trigger input voltage (min=1.0V max=3.5V)									
P60/KEYIN0/FTCI	26	KEY IN0	T ↑	I		I	I	Keep	Key matrix input 0 need pull high
P61/KEYIN1/FTOA	27	KEY IN1	T ↑	I		I	I	Keep H	Key matrix input 1 need pull high
P62/KEYIN2/FTIA	28	KEY IN2	T ↑	I		I	I	Keep	Key matrix input 2 need pull high
P63/KEYIN3/FTIB	29	KEY IN3	T ↑	I		I	I	Keep	Key matrix input 3 need pull high
P64/KEYIN4/FTIC	32	KEY IN4	T ↑	I		I	I	Keep	Key matrix input 4 need pull high
P65/KEYIN5/FTID	33	KEY IN5	T ↑	I		I	I	Keep	Key matrix input 5 need pull high
P66/KEYIN6/IRQ6	34	KEY IN6	T ↑	I		I	I	Keep	Key matrix input 6 need pull high
P67/KEYIN7/IRQ7	35	KEY IN7	T ↑	I		I	I	Keep	Key matrix input 7 need pull high
Port 7 TTL input voltage (input high min=2V, input low max=0.8V)									
P70/AN0	38	BAT VOLT1	T	I		I	I	T	Battery voltage measure
P71/AN1	39	BAT VOLT2	T	I		I	I	T	Battery voltage measure
P71/AN1	39	I_LIMIT	T	I		I	I	T	
P72/AN2	40	3V/PWR ok	T	I		I	I	T	Monitor system on/off state
P73/AN3	41	2.5V	T	I		I	I	T	
P73/AN3	41	LI/NIMH#	T	I		I	I	Keep	To differential 3S3P lithium ion battery and 9S NiMH battery
P74/AN4	42	BAT TEMP1	T	I		I	I	T	Battery thermister temperature
P75/AN5	43	BAT TEMP2	T	I		I	I	T	Battery thermister temperature
P75/AN5	43	VCC CORE	T	I		I	I	T	
P76/AN6/DA0	44	Charge-I_CTR	T	O		O	O	T	Charging current adjust
P77/AN7/DA1	45	BL ADJ	T	O		O	O	T	Backlight inverter brightness adjust

8575 N/B Maintenance

Continue to previous

Name	Pin	H8 Pin Definitions	During RESET	After RESET/OFF		ON	STANDBY		Function
Port 8 TTL input voltage (input high min=2V, input low max=0.8V)									
P80/HA0	93	ISA SA2	T	I		I	I	Keep	
P81/GA20	94	X(H8 A20GATE)	T	O		O	O	Keep H	CPU A20gate
P82/CS1	95	H8 KBCS#	T	I		I	I	Keep	IO port 60/64 chip select
P83/IOR	96	ISA IOR#	T	I		I	I	Keep	ISA I/O read#
P84/IRQ2/TXD1	97	ISA IOW#	T	I		I	I	Keep	ISA I/O write
P85/IRQ4/RXD1	98	H8 MCCS#	T	I		I	I	Keep	IO port 62/66 chip select
P86/IRQ5/SCK1	99	BAT CLK	T ↑	I/O		I/O	I/O	Keep	SM BUS clock need pull high 5→3V
Port 9 TTL input voltage (input high min=2V, input low max=0.8V)									
P90/IRQ2/ESC2	25	K/M CLK	T ↑	I/O		I/O	I/O	Keep	need pull high
P91/IRQ1/EIOW	24	M CLK	T ↑	I/O		I/O	I/O	Keep	need pull high
P92/IRQ0	23	H8/T CLK	T ↑	I/O		I/O	I/O	Keep	need pull high
P93/RD	22	K/M DATA	T ↑	I/O		I/O	I/O	Keep	need pull high
P94/WR	19	M DATA	T ↑	I/O		I/O	I/O	Keep	need pull high
P95/AS	18	H8/T DATA	T ↑	I/O		I/O	I/O	Keep	need pull high
P96/0	17	ENABKL	T ↑	I		I	I	T	Read H8 send A20gate status
P97/WAIT/SDA	16	BAT DATA	T ↑	I/O		I/O	I/O	Keep	SM BUS clock need pull high 5→3V

↑ Pull High
↓ Pull Low
5→3V Level shift

1.8 Appendix 3: 8575 Product Specifications

CPU	Intel Pentium 4 Processors Willamette/Northwood with mFCPGA2 Package, mPGA478 Socket Support up to Willamette P4 1.7GHz (Throttling) / Northwood above 2.0 GHz(Throttling) FSB 400MHz / PC 2100
Chipset	**SiS650 + SiS961**
L2 Cache	256KB
System BIOS	Flash EPROM (Include System BIOS and VGA BIOS) ACPI 1.0b; DMI 2.3.1 compliant
Memory	0MB SDRAM on board; Expandable to 1024MB Expandable with combination of optional 128MB/256MB/512MB memory Two 200-pin DDR SDRAM Memory Module, PC 2100/1600 specifications
ROM Drive	12.7mm Height 24X CD ROM Drive 8X DVD ROM Drive 8X4x24 CD-RW or above 8X8X4X24 Combo or above
HDD	2.5x9.5 mm height: 10/15/20/30GB; Support Ultra DMA 66/100 Reseller Exchangeable
Ext. FDD	Support External FDD w/z USB I/F; 3.5" Format for 720KB/1.2MB/1.44MB
Display	14.1”/ 15” XGA TFT display; Resolution: 1024 x 768 14.1”/15” SXGA+ TFT display; Resolution: 1280 x 1024 (P)

8575 N/B Maintenance

Continue to previous

Video Controller	Integrated in SiS650 Support Multi Monitor Ultra AGP REAL 256 2D/3D Graphic
Keyboard	19mm pitch/3.0mm stroke Windows Logo Key x 1; Application Key x 1
Button	5x Easy Start Buttons (functions defined by user)
Pointing Device	Glide pad with 2x buttons and 1x scroll button
PCMCIA	Type II or Type I x1 CardBus Support
Audio System	Sound Blaster Pro compatible Built-in mono microphone Support AC97 2.1 2X Speakers (1Watt each)
I/O Port	Bi-directional Parallel Port (EPP/ECP) x 1 Standard USB1.1 port x 2 RJ-11 port x 1 RJ-45 port x 1 IR port x1, complies with IrDA 1.1 DC input x 1 VGA monitor port x1 Audio-out x 1 (SPIDF) Mic-in x 1

8575 N/B Maintenance

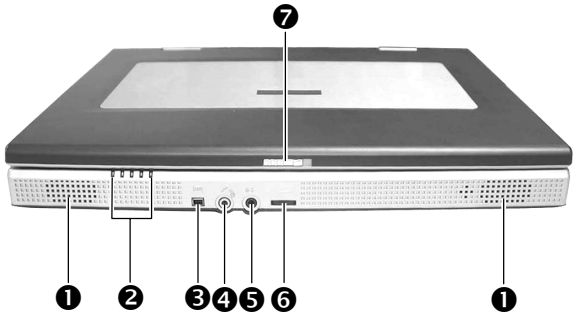
Continue to previous

I/O Port	Hardware Volume Control IEEE1394a Port x 1 S-Video Out Port x 1 (NTSC/PAL)
Communication	Built-in 56Kbps V.90 MDC modem Built-in 10/100 based-T LAN
Power Supply	9-cell Li-ion (2000mAH/3.7V) User swappable Battery Life: 1.5 hrs Support Power off charge : 3hr, 80% in 1.6Hrs Support Power on charge : 4hr~5.5hr
AC adapter	Universal AC adapter 90W ; Input: 100-240V, 50/60Hz AC
Dimensions	328 x 274 x 46~37
Weight	3.8
Accessories	Power Cord, AC Adapter, RJ-11 Phone Cable, Manual, System Driver CD-Title
Architecture	Support PC2001 specification, designed for Windows ME, Windows 2000 & Windows XP
Options	128MB/256MB/512MB DDR SDRAM, 9-cell Li-ION Battery Pack, AC Adapter w/o Power Cord, Notebook Carry Bag

2. System View and Disassembly

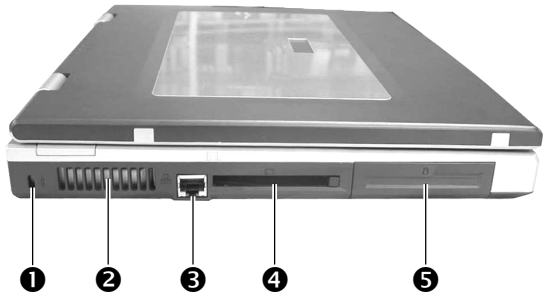
2.1 System View

2.1.1 Front View



❶ Stereo Speaker Set
❷ Device Indicators
❸ Mini IEEE1394 Connector
❹ External Microphone Jack
❺ Line Out Phone Jack
❻ Volume Control
❼ Top Cover Latch

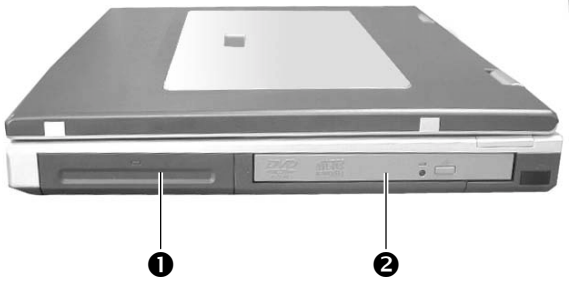
2.1.2 Left-side View



❶ Kensington Lock
❷ Ventilation Openings
❸ RJ-45 Connector
❹ PC Card Slot
❺ Hard Disk Drive

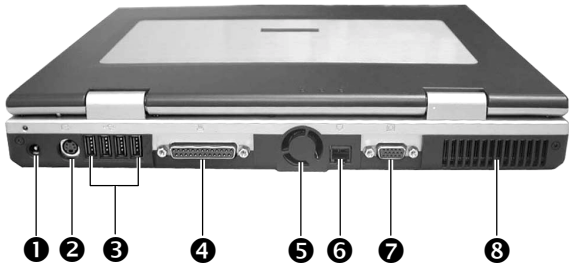
2.1.3 Right-side View

❶ Battery Pack
❷ CD-ROM/DVD-ROM Drive



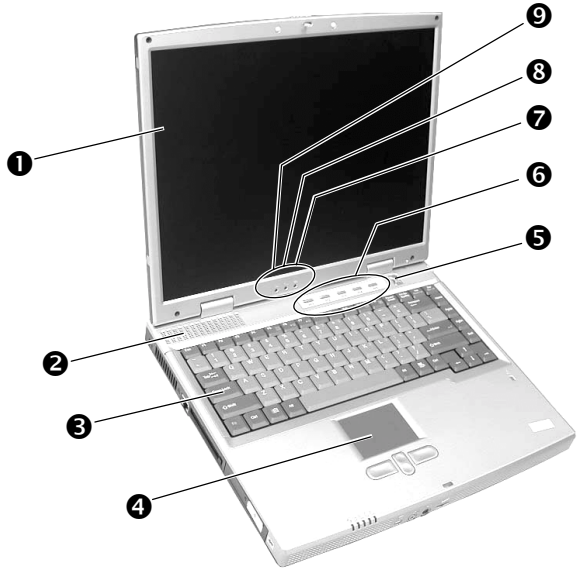
2.1.4 Rear View

❶ Power Connector
❷ S-Video Output Connector
❸ USB Ports
❹ Parallel Port
❺ D/D Fan
❻ RJ-11 Connector
❼ VGA Port
❽ Ventilation Openings



8575 N/B Maintenance

2.1.5 Top-open View

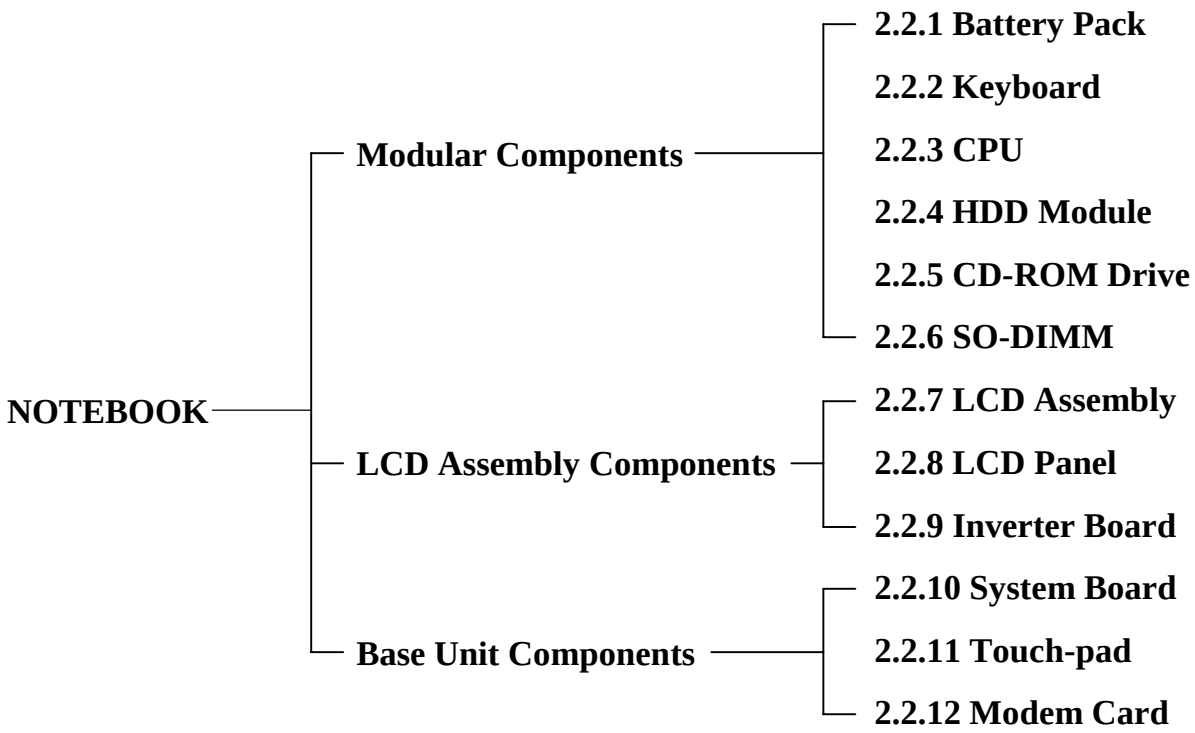


❶ LCD Screen
❷ Microphone
❸ Keyboard
❹ Touch Pad
❺ Power Button
❻ Easy Start Buttons
❼ Battery Charge Indicator
❽ Battery Power Indicator
❾ AC Power Indicator

2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the release lever to the "unlock" ( ) position (❶), then sliding and holding the release lever outwards while pull the battery pack out of the compartment (❷). (Figure 2-1)

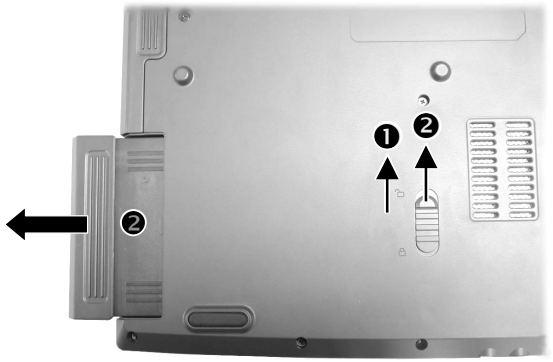


Figure 2-1 Remove the battery pack

Reassembly

1. Push the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" ( ) position.

2.2.2 Keyboard

Disassembly

1. Open the top cover.
2. Insert a small rod, such as a straightened paper clip, into the eject hole near the power connector of the notebook. (Figure 2-2)
3. Push the rod firmly and slide the easy start buttons cover to the left (❶). Then lift the easy start buttons cover up from the left side (❷). (Figure 2-3)

Figure 2-2 Insert a rod easy to remove

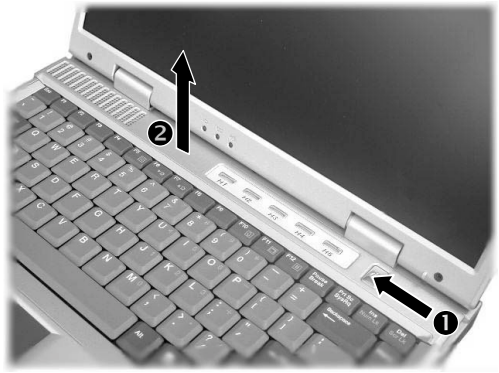


Figure 2-16 Remove easy start buttons cover

3. Remove three screws fastening keyboard on the base unit cover. (Figure 2-4)
4. Slightly lift up the keyboard and disconnect the cable from the system board to detach the keyboard. (Figure 2-5)

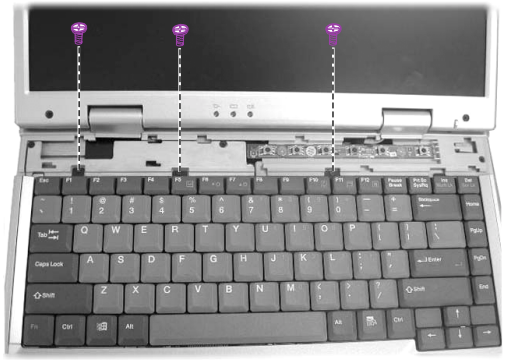


Figure 2-4 Remove three screws

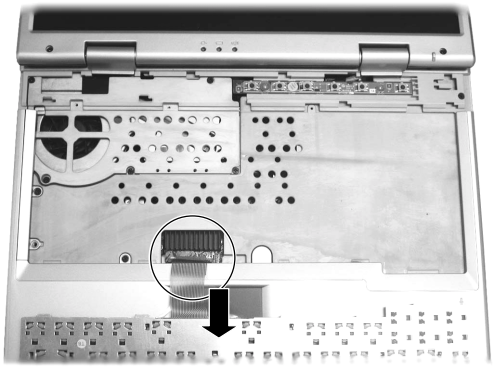


Figure 2-5 Remove keyboard

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place with three screws.
2. Replace the easy start buttons cover.

2.2.3 CPU

Disassembly

1. Remove the easy start buttons cover and keyboard to access the CPU compartment. (See section 2.2.2 Disassembly)
2. Remove seven screws fastening the heatsink cover and the rail. (Figure 2-6)
3. Remove three screws fastening the heatsink. (Figure 2-7)

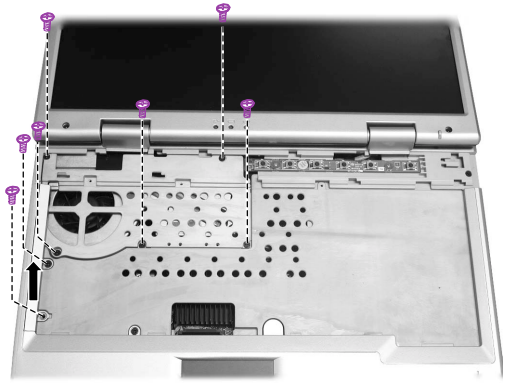


Figure 2-6 Remove the cover and rail

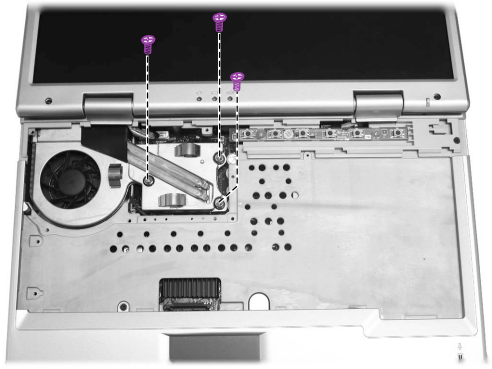


Figure 2-7 Remove the heatsink

4. Disconnect the fan's power cord from the system board, then lift up the heatsink. (Figure 2-8)
5. Push the lever to the right. Then lift up the lever to the vertical position. Finally, Remove the existing CPU. (Figure 2-9)

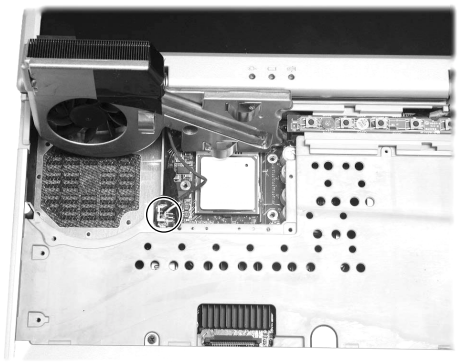


Figure 2-8 Remove the fan's power cord

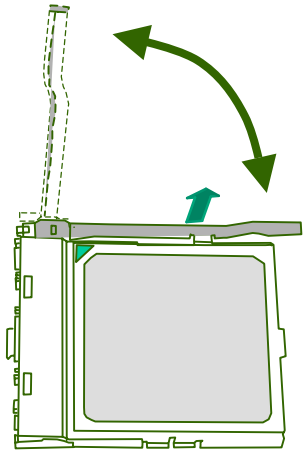


Figure 2-9 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Place the lever back to the horizontal position and push the lever to the left.
2. Connect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with four screws.
3. Replace the keyboard .Then replace easy start buttons cover.

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove one screw and slide the HDD module out of the compartment. (Figure 2-10)
3. Remove six screws to separate the hard disk drive from the metal shield. (Figure 2-11)

Figure 2-10 Remove HDD module

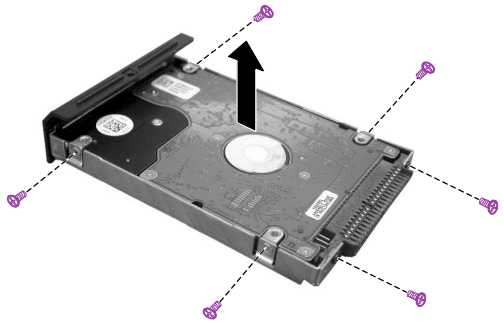


Figure 2-11 Disassemble the hard disk

Reassembly

1. To install the hard disk drive, place it in the bracket and secure with six screws.
2. Slide the HDD module into the compartment and secure with one screw.

2.2.5 CD-ROM Drive

Disassembly

1. Carefully put the notebook upside down.
2. Remove one screw fastening the CD/DVD-ROM drive. Then hold the CD/DVD-ROM drive and slide it outwards carefully. (Figure 2-12)

Figure 2-12 Remove one screw to loose the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment.
2. Secure the CD/DVD-ROM drive with one screw.

2.2.6 SO-DIMM

Disassembly

1. Carefully put the notebook upside down.
2. Remove seven screws to access the SO-DIMM socket. (Figure 2-13)
3. Full the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-14)

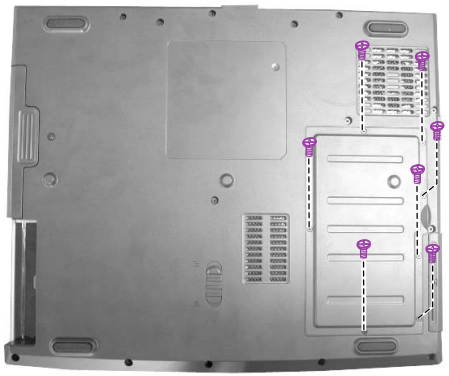


Figure 2-13 Remove the SO-DIMM cover

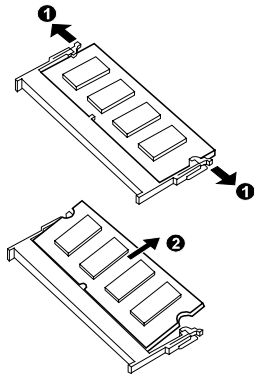


Figure 2-14 Remove the SO-DIMM

Reassembly

1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the OS-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into cover.
2. Replace the SO-DIMM cover.
3. Replace seven screws to fasten the SO-DIMM socket cover.

2.2.7 LCD

Disassembly

1. Open the top cover. Remove easy start buttons cover, keyboard, and heatsink . (See section 2.2.2 and 2.2.3 Disassembly)
2. Remove the two hinge covers and remove two screws fastening the easy start button board.(Figure 2-15)
3. Disconnect the LCD cables from the system board, and remove four screws of the hinges. Now you can separate the LCD assembly from the base unit. (Figure 2-16)

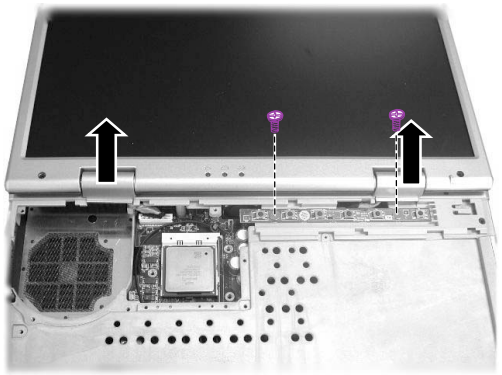


Figure 2-15 Remove the LCD hinge cover and button board

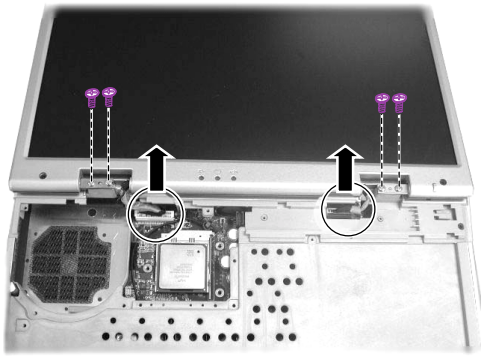


Figure 2-16 Remove cables and screws to separate LCD

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges.
2. Reconnect the LCD cable connectors to the system board.
3. Fit the easy start button board and secure with tow screws.
4. Replace two hinge cover, the heatsink, keyboard and easy start buttons cover.

2.2.8 LCD Panel

Disassembly

1. Remove the LCD assembly. (See section 2.2.7 Disassembly)
2. Remove the four rubber pads and two screws on the lower part of the panel. (figure 2-17)
3. Insert a flat screwdriver to the lower part of the frame and gently pry the frame out. Repeat the process until the frame is completely separated from the housing.
4. Remove the two screws on two sides and two screws on the lower part of the LCD panel, and disconnect the cable from the inverter board. (figure 2-18)

Figure 2-17 Remove LCD frame

Figure 2-18 Remove LCD panel

Reassembly

1. Fit the LCD panel back into place and secure with four screws, and reconnect the cable to the inverter board.
2. Fit the LCD frame back into the housing and replace the four screws and four rubber pads.
3. Replace the LCD assembly. (See section 2.2.7 Reassembly)

2.2.9 Inverter Board

Disassembly

1. Remove the LCD assembly and detach the LCD panel. (see instructions in previous two sections)
2. To remove the inverter board on the bottom side of the LCD assembly, disconnect the cable and remove one screw. (figure 2-19)

Figure 2-19 Remove the inverter board

Reassembly

1. Fit the inverter board back into place and secure with one screw.
2. Reconnect the cable.
3. Replace the LCD frame. (See section 2.2.8 Reassembly)
4. Replace the LCD assembly. (See section 2.2.7 Reassembly)

2.2.10 System Board

Disassembly

1. Remove the battery pack, keyboard, CPU, HDD module, CD/DVD-ROM drive and LCD assembly. (See section 2.2.1 to 2.2.5 and 2.2.7 Disassembly)
2. Remove fourteen screws on the bottom of the notebook. (Figure 2-20)
3. Remove nine screws fastening the base unit cover. (figure 2-21)

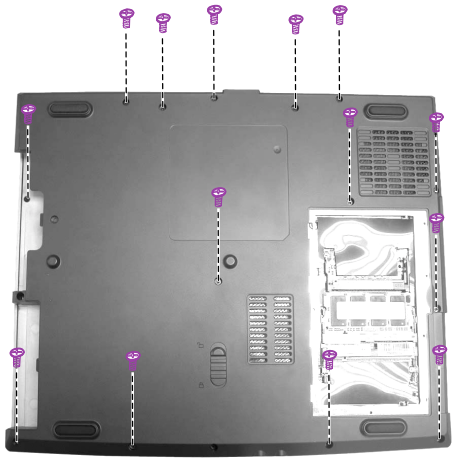


Figure 2-20 Remove the bottom

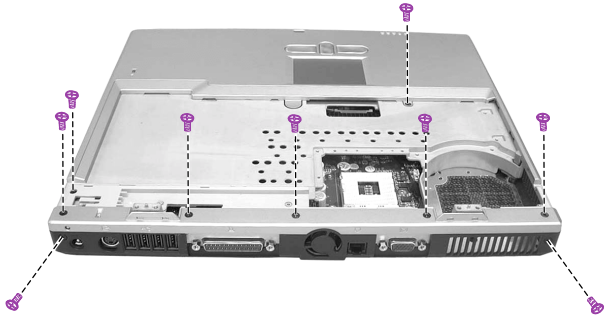


Figure 2-21 Remove the speaker assembly

4. Lift up the base unit cover and disconnect the touch pad cord. (Figure 2-22)
5. Remove the four screws fastening the base unit. (Figure 2-23)

Figure 2-22 Remove the base unit cover

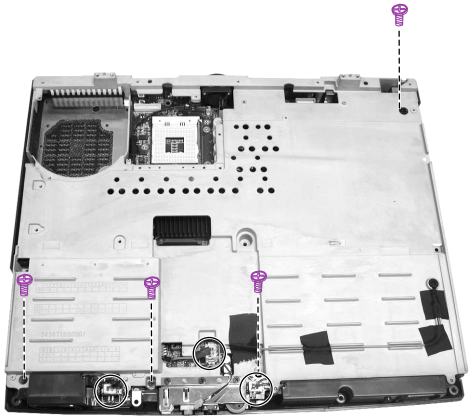


Figure 2-23 Remove the metal shield

6. Carefully put the notebook upside down.
7. Remove four screws fastening the system board and disconnect the cables. (Figure 2-24)
8. Lift up the system board and disconnect cable. Now you can remove the system board. (Figure 2-25)

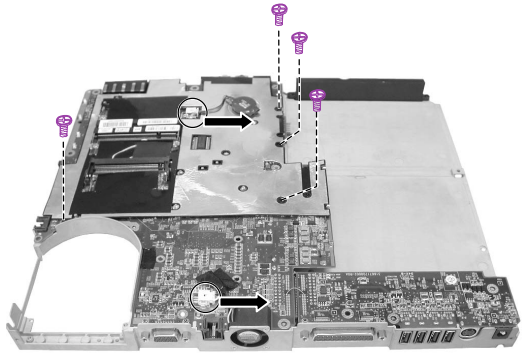


Figure 2-24 Remove the screws and disconnect the cable

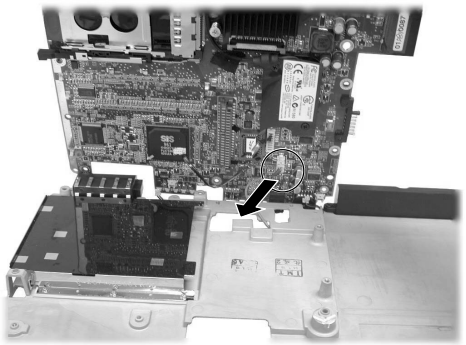


Figure 2-25 Remove the system board

Reassembly

1. Reconnect the cable to system board.
2. Replace four screws fasten the system board.
3. Reconnect one cable of system board fan and one cable of little battery to system board.
4. Replace four screws fasten the base unit.
5. Reconnect the touch pad cord.
6. Replace the base unit cover and secure with nine screws
7. Carefully put the notebook upside down. Then replace the bottom frame and secure with fourteen screws.
8. Replace the battery pack, LED panel, keyboard, CPU, HDD module, CD/DVD-ROM drive and LCD assembly.

2.2.11 Touch-pad

Disassembly

1. Remove the base unit cover. (See steps 1-6 in section 2.2.10 Disassembly.)
2. Remove the eight screws to lift up the touch pad holder and touch pad panel. (Figure 2-26)

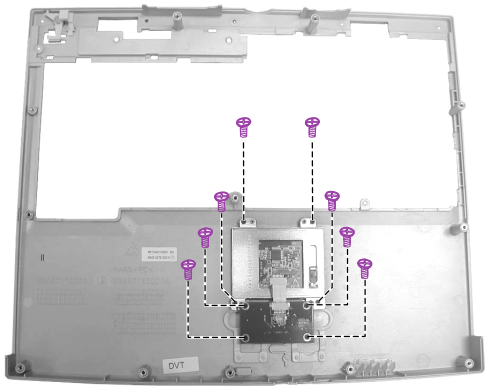


Figure 2-26 Remove the touch-pad

Reassembly

1. Replace the touch-pad holder and touch-pad panel, and secure with eight screws.
2. Assemble the base unit cover. (See section 2.2.10 Reassembly)

2.2.12 Modem Card

Disassembly

1. Remove the battery pack, keyboard, CPU, HDD module, CD/DVD-ROM drive, and LCD assembly. (See section 2.2.1 to 2.2.5 and 2.2.7 Disassembly)
2. Disassemble the notebook to access the system board. (See section 2.2.10 Disassembly)
3. Remove the two screws fastening the modem card,and then disconnect the cable from system board. (Figure 2-27)

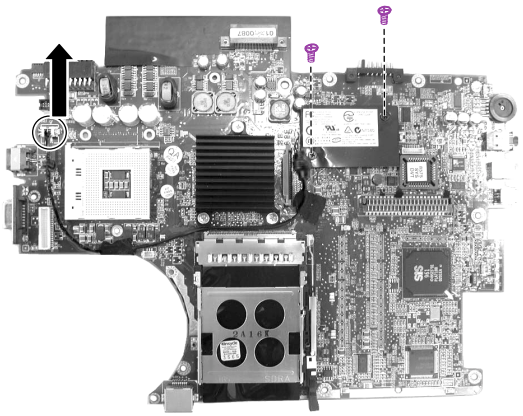


Figure 2-27 Remove the Modem card

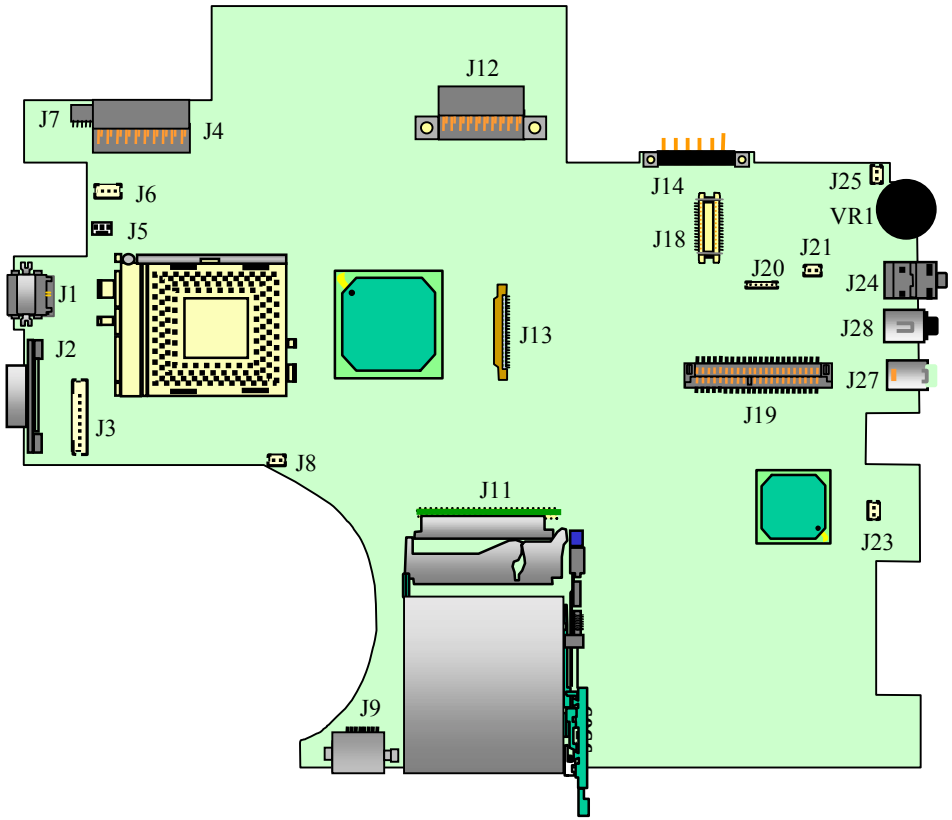
Reassembly

1. Reconnect the cable to the modem card and secure the modem card with two screws.
2. Assemble the notebook. (See section 2.2.10 Reassembly)

8575 N/B Maintenance

3. Definition & Location of Connectors / Switches

3.1 Mother Board – A-1

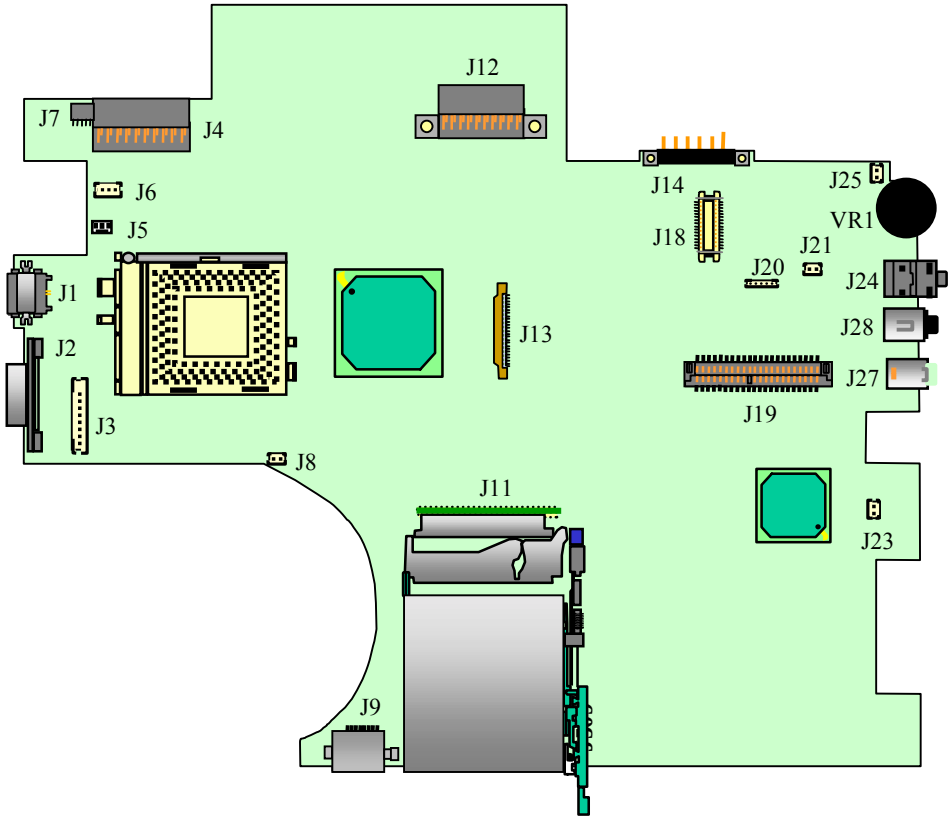


- J1 : Modem Connector (RJ11)
- J2 : External VGA Connector
- J3 : LCD Connector
- J4 : D/D Connector
- J5 : MDC Jump Wire Connector
- J6 : Easy Start Buttons Connector
- J7 : MISC Connector
- J8 : Fan Connector
- J9 : LAN Connector (RJ45)
- J11 : PC Card Socket
- J12 : Secondary IDE Connector
- J13 : Internal Keyboard Connector
- J14 : Battery Connector

8575 N/B Maintenance

3. Definition & Location of Connectors / Switches

3.1 Mother Board – A-2

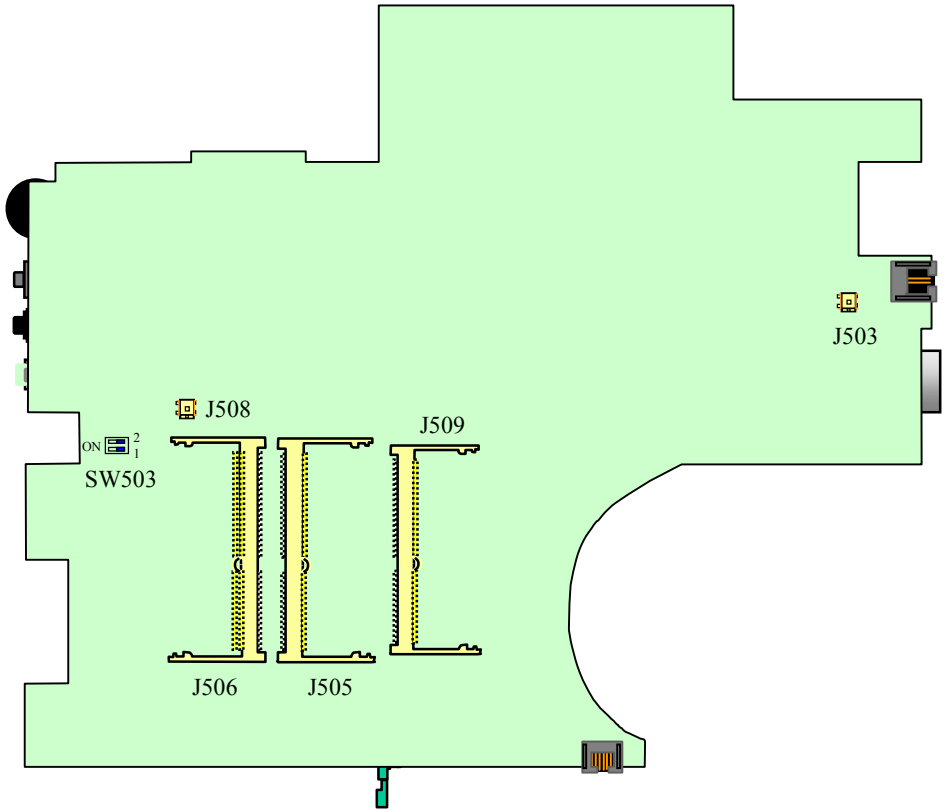


- **J18 : MDC Connector**
- **J19 : Primary IDE Connector**
- **J20 : Touch-pad Connector**
- **J21 : Internal Micro Phone Jack**
- **J23 : L Speaker Connector**
- **J24 : Line Out Phone Jack**
- **J25 : R Speaker Connector**
- **J27 : IEEE1394 Port**
- **J28 : External Microphone Jack**
- **VR1 : Volume Control**

8575 N/B Maintenance

3. Definition & Location of Connectors / Switches

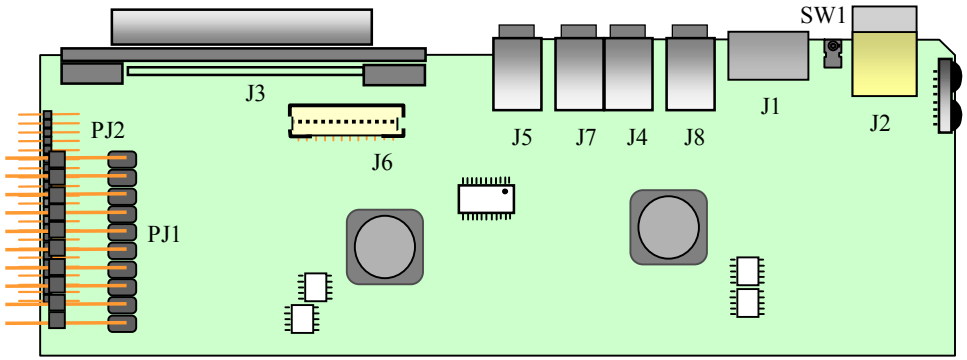
3.1 Mother Board – B



- **J503 : Fan Connector**
- **J505 : 200-pin expansion DDR SDRAM Socket**
- **J506 : 200-pin expansion DDR SDRAM Socket**
- **J508 : CMOS Battery Connector**
- **J509 : Mini PCI Socket**
- **SW503 : Country Selection for Keyboard**

3. Definition & Location of Connectors / Switches

3.2 DC Power Board - A

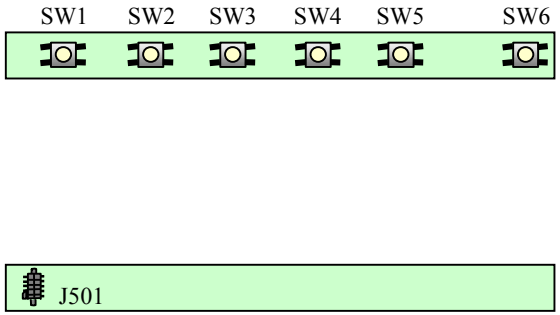


- **J1 : TV Out Jack**
- **J2 : Power Jack (AC adapter)**
- **J3 : Parallel Port Connector**
- **J4 : USB Port Connector**
- **J5 : USB Port Connector**
- **J6 : Inverter Board Connector**
- **J7 : USB Port Connector**
- **J8 : USB Port Connector**
- **PJ1 : D/D Connector**
- **PJ2 : MISC Connector**
- **SW1 : Cover Switch**

8575 N/B Maintenance

3. Definition & Location of Connectors / Switches

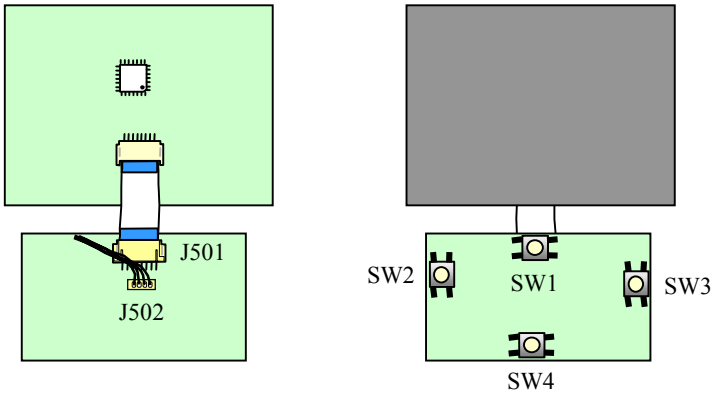
3.3 ESB Board – A,B



- **J501 : Easy Start Button Connector**
- **SW1 : Programmable Easy Start Button Switch**
- **SW2 : Programmable Easy Start Button Switch**
- **SW3 : Programmable Easy Start Button Switch**
- **SW4 : Programmable Easy Start Button Switch**
- **SW5 : Programmable Easy Start Button Switch**
- **SW6 : Programmable Easy Start Button Power Switch**

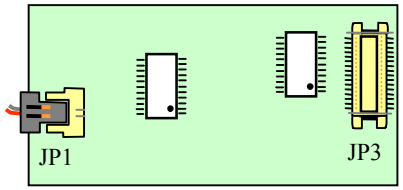
3. Definition & Location of Connectors / Switches

3.4 Touch-pad – A,B



- **J501 : Touch-pad Board to Touch-pad Connector**
- **J502 : Touch-pad Board to Main Board Connector**
- **SW1 : Scroll Up Button Switch**
- **SW2 : Left Button Switch**
- **SW3 : Right Button Switch**
- **SW4 : Scroll Down Button Switch**

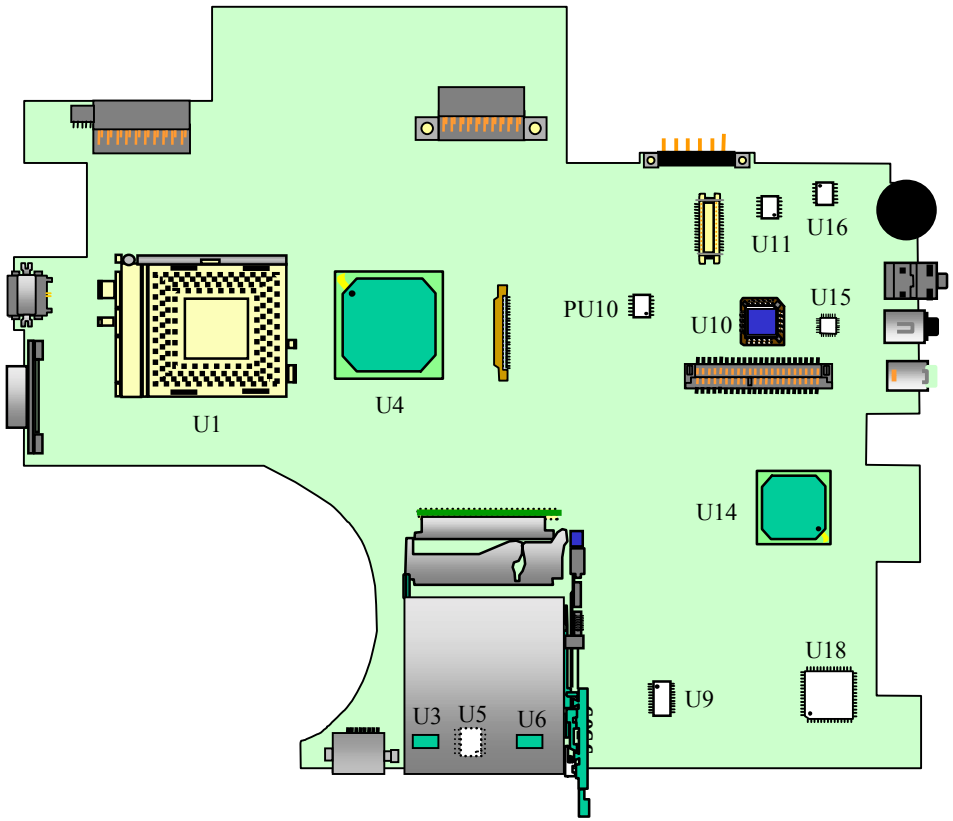
3.5 Daughter Board -A



- **JP1 : MDC Jump Wire Connector**
- **JP3 : MDC/LAN Transfer Board to M/B Connector**

4. Definition & Location of Major Components

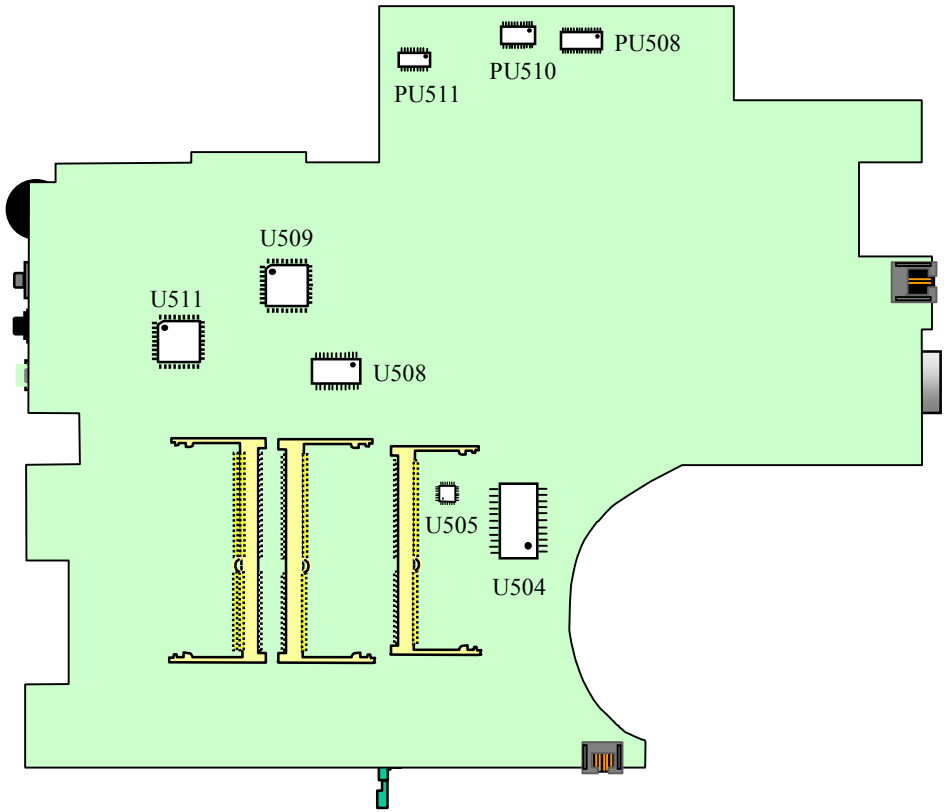
4.1 Mother Board - A



- U1 : Intel Pentium 4 Processor mPGA478 Socket
- U3 : LF-H80P LAN Buffer
- U4 : SiS650 IGUI Host/Memory Controller
- U5 : ISC1893Y LAN Controller
- U6 : PCI1410GGU PCMCIA Controller
- U9 : ICS93722 Clock Buffer
- U10 : Flash ROM
- U11 : SN74CBTD3384 Level Shift
- U14 : SiS961 MuTIOL Media I/O Controller
- U15 : ALC201 Audio CODEC
- U16 : TPA0202 Audio Amplifier
- U18 : uPD72872 IEEE 1394 Controller
- PU10 : CM8500 1.25V Generator

4. Definition & Location of Major Components

4.1 Mother Board - B



- **U504 : SiS301LV/Chrontel CH7019**
- **U505 : TPS2211 PC Card Slot Power Switch**
- **U508 : ICS952001 Clock Generator**
- **U509 : H8/F3437 Micro Controller**
- **U511 : PC87393 Super I/O**
- **PU508 : LTC1709EG-7 CPU Power Generator**
- **PU510 : LTC3707 1.8V/2.5V Generator**
- **PU511 : TL594C PWM**

5. Pin Descriptions of Major Components

5.1 Intel Pentium 4 Processor mPGA478 Socket

Name	Type	Description
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2 36 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Pentium 4 processor in the 478-pin package system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.

Signals	Associated Strobe
REQ[4:0]#, A[16:3]#	**ADSTB0#**
A[35:17]#	**ADSTB1#**

Name	Type	Description
AP[1:0]#	Input/ Output	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#,A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus agents. The following table defines
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V CROSS .
BINIT#	Input/ Output	BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Request Signals	subphase 1	subphase 2
A[35:24]#	**AP0#**	**AP1#**
A[23:3]#	**AP1#**	**AP0#**
REQ[4:0]#	**AP1#**	**AP0#**

5.1 Intel Pentium 4 Processor mPGA478 Socket

Name	Type	Description
BPM[5:0]#	Input/ Output	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. Please refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more detailed information. **These signals do not have on-die termination. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for termination requirements.**
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	Input/ Output	BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this pin is sampled to determine the agent ID = 0. **This signal does not have on-die termination and must be terminated.**
BSEL[1:0]	Output	The BCLK[1:0] frequency select signals BSEL[1:0] are used to select the processor input clock frequency. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The Pentium 4 processor in the 478-pin package operates currently at a 400 MHz system bus frequency (100 MHz BCLK[1:0] frequency).
COMP[1:0]	Analog	COMP[1:0] must be terminated on the system board using precision resistors. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for details on implementation.

Name	Type	Description
D[63:0]#	Input/ Output	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#. **Quad-Pumped Signal Groups** Data Group / DSTBN#/ DSTBP# / DBI# D[15:0]# / 0 / 0 D[31:16]# / 1 / 1 D[47:32]# / 2 / 2 D[63:48]# / 3 / 3 Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBI[3:0]#	Input/ Output	DBI[3:0]# are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DBI[3:0] Assignment To Data Bus** Bus Signal / Data Bus Signals DBI3# / D[63:48]# DBI2# / D[47:32]# DBI1# / D[31:16]# DBI0# / D[15:0]#
DBR#	Output	DBR# is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.

5.1 Intel Pentium 4 Processor mPGA478 Socket

Name	Type	Description
DBSY#	Input/ Output	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus isreleased after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.
DEFER#	Input	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor system bus agents.
DP[3:0]#	Input/ Output	DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus gents.
DSTBN[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe D[15:0]#, DBI0# — DSTBN0# D[31:16]#, DBI1# — DSTBN1# D[47:32]#, DBI2# — DSTBN2# D[63:48]#, DBI3# — DSTBN3#
DSTBP[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe D[15:0]#, DBI0# — DSTBP0# D[31:16]#, DBI1# — DSTBP1# D[47:32]#, DBI2# — DSTBP2# D[63:48]#, DBI3# — DSTBP3#
FERR#	Output	FERR# (Floating-point Error) is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*-type floating-point error reporting.
GTLREF	Input	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 Vcc. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more information.

Name	Type	Description
HIT# **HITM#**	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. This signals does not have on-die termination.
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error.IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITPCLKOUT[1:0]	Output	The ITPCLKOUT[1:0] pins do not provide any output for the Pentium® 4 processor in the 478-pin package.
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.

5.1 Intel Pentium 4 Processor mPGA478 Socket

Name	Type	Description
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: Enabled or disabled. Asserted, if configured, for internal errors along with IERR#. Asserted, if configured, by the request initiator of a bus transaction after it observes an error. Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, please refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*.
PROCHOT#	Output	PROCHOT# will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. .

Name	Type	Description
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after VCC and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. This signal does not have on-die termination and must be terminated on the system board.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.

5.1 Intel Pentium 4 Processor mPGA478 Socket

Name	Type	Description
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for a details on parity checking of these signals.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If the BCLK input is stopped while in the Sleep state the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also knownas the Test Access Port).

Name	Type	Description
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[12:8] **TESTHI[5:0]**	Input	TESTHI[12:8] and TESTHI[5:0] must be connected to a VCC power source through a resistor for proper processor operation.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	Output	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C.Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (VCC) must be removed following the assertion of THERMTRIP#. Once activated, THERMTRIP# remains latched until RESET# is asserted. While the assertion of the RESET# signal will de-assert THERMTRIP# , if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted after RESET# is de-asserted.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.1 Intel Pentium 4 Processor mPGA478 Socket

Name	Type	Description
VCCIOPLL	Input	VCCIOPLL provides isolated power for internal processor system bus PLLs. Follow he guidelines for VCCA, and refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.
VCCSENSE	Output	VCCSENSE is an isolated low impedance connection to processor core power(VCC). It can be used to sense or measure power near the silicon with little noise.
VCCVID	Input	There is no imput voltage requirement for VCCVID for designs intended tosupport only the Pentium 4 processor in the 478-pin package. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more information.
VID[4:0]	Output	VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages (Vcc). These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support processor voltage specification variations. The power supply must supply the voltage that is requested by these pins, or disable itself.
VSSA	Input	VSSA is the isolated ground for internal PLLs.
VSSSENSE	Output	VSSSENSE is an isolated low impedance connection to processor core Vss. It can be used to sense or measure ground near the silicon with little noise
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.2 SiS650 IGUI Host/Memory Controller

Host BUS Interface

Name	Pin Attr	Signal Description
CPUCLK **CPUCLK#**	I 0.71V – M	**Host differential clock input.**
CPURST#	O 1.2~1.85V – M	**Host Bus Reset:** CPURST# is used to keep all the bus agents in the same initial state before valid cycles issued.
CPUPWRGD#	O 1.2~1.85V – M	**CPUPWRGD#** is used to inform CPU that main power is stable
ADS#	I/O 1.2~1.85V – M	**Address Strobe :** Address Strobe is driven by CPU or SiS650 to indicate the start of a CPU bus cycle.
HADSTB[1:0]#	1.2~1.85V – M	**Source synchronous address strobe** used to latch HREQ[4:0]# & HA[31:3]# at both falling and rising edge. HREQ[4:0]# & HA[16:3]# are latched by HASTB0# HA[31:17] are latched by HASTB1#
HREQ[4:0]#	I/O 1.2~1.85V – M	**Request Command:** HREQ[4:0]# are used to define each transaction type during the clock when ADS# is asserted and the clock after ADS# is asserted.
HA[31:3]#	I/O 1.2~1.85V – M	**Host Address Bus**
BREQ0#	O 1.2~1.85V – M	**Symmetric Agent Bus Request:** BREQ0# is driven by the symmetric agent to request for the bus.
BPRI#	O 1.2~1.85V – M	**Priority Agent Bus Request:** BPRI# is driven by the priority agent that wants to request the bus. BPRI# has higher priority than BREQ0# to access a bus.
BNR#	I/O 1.2~1.85V – M	**Block Next Request:** This signal can be driven asserted by any bus agent to block further requests being pipelined.
HLOCK#	I 1.2~1.85V – M	**Host Lock** : CPU asserts HLOCK# to indicate the current bus cycle is locked.
HIT#	I/O 1.2~1.85V – M	**Keeping a Non-Modified Cache Line**
HITM#	I/O 1.2~1.85V – M	**Hits a Modified Cache Line:** Hit Modified indicates the snoop cycle hits a modified line in the L1/L2 cache of CPU.
DEFER#	O 1.2~1.85V – M	**Defer Transaction Completion:** r defer response to host bus.

Host BUS Interface Continue

Name	Pin Attr	Signal Description
RS[2:0]#	O 1.2~1.85V – M	**Response Status:** RS[2:0]# are driven by the response agent to indicate the transaction response type. The following shows the response type. RS[2:0] Response 000 Idle State 001 Retry 010 Defer 011 Reserved 100 Reserved 101 No data 110 Implicit Write-back 111 Normal Data
HTRDY#	O 1.2~1.85V – M	**Target Ready:** During write cycles, response agent will drive TRDY# to indicate it is ready to accept data.
DRDY#	I/O 1.2~1.85V – M	**Data Ready:** DRDY# is driven by the bus owner whenever the data is valid on the bus.
DBSY#	I/O 1.2~1.85V – M	**Data Bus Busy:** Whenever the data is not valid on the bus with DRDY# is deserted, DBSY# deasserted to hold the bus.
HD[63:0]#	I/O 1.2~1.85V – M	**Data Bus Busy:** Whenever the data is not valid on the bus with DRDY# is deserted, DBSY# deasserted to hold the bus.
DBI[3:0]#	I/O 1.2~1.85V – M	**Dynamic Bus Inversion:** An active DBI# will invert it's corresponding data group signals. DBI0# is referenced by HD[15:0], DBI1# is referenced by HD[31:16] DBI2# is referenced by HD[47:32] DBI3# is referenced by HD[63:48]
HDSTBP[3:0]#	I/O 1.2~1.85V – M	**Source synchronous data strobe** used to latch data at falling edge HD[15:0], DBI0# are latched by HDSTBP0# HD[31:16], DBI1# are latched by HDSTBP1# HD[47:32], DBI2# are latched by HDSTBP2# HD[63:48], DBI3# are latched by HDSTBP3#
HDSTBN[3:0]#	I/O 1.2~1.85V– M	**Source synchronous data strobe** used to latch data at falling edge HD[15:0], DBI0# are latched by HDSTBN0# HD[31:16], DBI1# are latched by HDSTBN1# HD[47:32], DBI2# are latched by HDSTBN2# HD[63:48], DBI3# are latched by HDSTBN3#
HNCOMP	I M	**GTL N-MOS Compensation Input**

5.2 SiS650 IGUI Host/Memory Controller

Host BUS Interface Continue

Name	Pin Attr	Signal Description
HPCOMP	I M	**GTL P-MOS Compensation Input**
HVREF[4:0] **HNCOMPVREF**	I M	**AGTL+ I/O reference voltage**

DRAM Controller

Name	Pin Attr	Signal Description
SDCLK	I 3.3V - M	**SDRAM Clock Input**
SDRCLKI	I 2.5V/3.3V - M	**SDRAM Read Clock Input**
FWDSDCLKO	O 2.5V/3.3V – M	**SDRAM Forward Clock Output**
MA[14:0]	O 2.5V/3.3V - M	**System Memory Address Bus**
SRAS#	O 2.5V/3.3V - M	**SDRAM Row Address Strobe**
SCAS#	O 2.5V/3.3V - M	**SDRAM Column Address Strobe**
SWE#	O 2.5V/3.3V - M	**SDRAM Write Enable**
CS[5:0]# **CSB[5:0]#**	O 2.5V/3.3V - M	**SDRAM Chip Select** **CSB[5:0] multiplexed with DQS[5:0]**
DQM[7:0]#	O 2.5V/3.3V - M	**SDRAM Input/Output Data Mask**
DQS[7:0]	I/O 2.5V/3.3V - M	**DDR Data Strobe**
MD[63:0]	I/O 2.5V/3.3V - M	**System Memory Data Bus**
CKE[5:0]	O (open-drain) 2.5V/3.3V – AUX	**SDRAM Clock Enable**
S3AUXSW# **(CKE6)**	O (open-drain) 2.5V/3.3V - AUX	**Aux power switch for ACPI-S3 state, low active.**
DDRVREF[A:B]	I M	**DDR I/O Reference Voltage**

SiS MuTIOL Interface

Name	Pin Attr	Signal Description
ZCLK	I 3.3V - M	**SiS MuTIOL Connect**
ZUREQ/ZD **REQ**	I/O 1.8V - M	**SiS MuTIOL Connect Control pins**
ZSTB[1:0]	I/O 1.8V - M	**SiS MuTIOL Connect Strobe**
ZSTB[1:0]#	I/O 1.8V - M	**Strobe Compliment**
ZAD[15:0]	I/O 1.8V - M	**I/O** **1.8V - M**
ZVREF	I M	**SiS MuTIOL Connect Reference Voltage**
ZCMP_N	I M	**N-MOS Compensation Input**
ZCMP_P	I M	**P-MOS Compensation Input**

SiS MuTIOL Interface Continue

Name	Pin Attr	Signal Description
AGPCLK	I 3.3V – M	**AGP Clock**
AFRAME#	I/O 1.5V/3.3V - M	**AGP Frame#**
AIRDY#	I/O 1.5V/3.3V - M	**AGP Initiator Ready**
ATRDY#	I/O 1.5V/3.3V - M	**AGP Target Ready**
ASTOP#	I/O 1.5V/3.3V - M	**AGP Stop#**
ADEVSEL#	I/O 1.5V/3.3V - M	**AGP Device Select**
ASERR#	I 1.5V/3.3V - M	**AGP System Error**
AREQ#	I 1.5V/3.3V - M	**AGP Bus Request**
AGNT#	O 1.5V/3.3V - M	**AGP Bus Grant**
AAD[31:0]	I/O 1.5V/3.3V - M	**AGP Address/Data Bus**

5.2 SiS650 IGUI Host/Memory Controller

SiS MuTIOL Interface

Name	Pin Attr	Signal Description
AC/BE[3:0]	I/O 1.5V/3.3V - M	**AGP Command/Byte Enable**
APAR	I/O 1.5V/3.3V - M	**AGP Parity**
ST[2:0]	O 1.5V/3.3V - M	**AGP Status Bus**
PIPE#	I 1.5V/3.3V - M	**AGP Pipeline Request**
SBA[7:0]	I/O 1.5V/3.3V - M	**Side Band Address**
RBF#	I 1.5V/3.3V - M	**Read Buffer Full**
WBF#	I 1.5V/3.3V - M	**Write Buffer Full**
AD_STB[1:0]	I/O 1.5V/3.3V - M	**AD Bus Strobe**
AD_STB[1:0]#	I/O 1.5V/3.3V - M	**AD Bus Strobe Compliment**
SB_STB	I 1.5V/3.3V - M	**Side Band Strobe**
SB_STB#	I 1.5V/3.3V - M	**Side Band Strobe Compliment**

Stereo Glasses Interface

Name	Pin Attr	Signal Description
CSYNC	O 3.3V - M	**Stereo Clock**
RSYNC	O 3.3V - M	**Stereo Right**
LSYNC	O 3.3V - M	**Stereo Left**

VB Interface

Name	Pin Attr	Signal Description
VBCLK	I 1.8V/3.3V - M	**Channel B/A Clock Input** VBCLK multiplexed with SBA0
VBHCLK	O 1.8V/3.3V – M	**VB Programming Interface Clock** VBHCLK multiplexed with RBF#
VBCAD	I/O 1.8V/3.3V – M	**VB Programming Interface Data** VBCAD multiplexed with AREQ#
VBCTL[1:0]	O 1.8V/3.3V - M	**VB Data Control** VBCTL[1:0] multiplexed with AAD[29:28]
VGPIO[3:2]	I/O 3.3V - M	**VB GPIO pins** VGPIO[3:2] multiplexed with PIPE#/WBF#
VBHSYNC	I/O 1.8V/3.3V - M	**Channel B H-Sync** VBHSYNC multiplexed with AAD30
VBVSYNC	I/O 1.8V/3.3V - M	**Channel B V-Sync** VBVSYNC multiplexed with AAD31
VBDE	I/O 1.8V/3.3V - M	**Channel B Data Valid** VBDE multiplexed with AAD27
VBGCLK	I/O 1.8V/3.3V - M	**Channel B Clock Output.** This clock is used to trigger dual edge data transfer. Perfect duty cycle is required. VBGCLK multiplexed with AD_STB1
VBD[11:0]	I/O 1.8V/3.3V - M	**Channel B Data** VBD[11:0] multiplexed with AAD
VAHSYNC	I/O 1.8V/3.3V - M	**Channel A H-Sync** VAHSYNC multiplexed with AAD18
VAVSYNC	I/O 1.8V/3.3V - M	**Channel A V-Sync** VAVSYNC multiplexed with AAD17
VADE	I/O 1.8V/3.3V - M	**Channel A Data Valid** VADE multiplexed with AAD16
VAGCLK	I/O 1.8V/3.3V - M	**Channel A Clock Output.** This clock is used to trigger dual edge data transfer. Perfect duty cycle is required. VAGCLK multiplexed with AD_STB0
VAGCLK#	I/O 1.8V/3.3V - M	**Channel A Differential Clock Output. (**To support Chrontel). VAGCLK# multiplexed with AD_STB0#
VAD[11:0]	I/O 1.8V/3.3V - M	**Channel A Data** VAD[11:0] multiplexed with AAD

5.2 SiS650 IGUI Host/Memory Controller

VGA Interface

Name	Pin Attr	Signal Description
VOSCI	I 3.3V - M	**14.318 Reference Clock Input**
HSYNC	O 3.3V - M	**Horizontal Sync**
VSYNC	O 3.3V - M	**Vertical Sync**
INTA#	O 3.3V - M	**Internal VGA Interrupt Pin**
VGPIO[1:0]	I/O 3.3V - M	**Internal VGA GPIO pins**
VCOMP	AI Analog - M	**Compensation Pin**
VRSET	AI Analog - M	**Reference Resistor**
VVBWN	AI Analog - M	**Voltage Reference**
ROUT	AO Analog - M	**Red Signal Output**
GOUT	AO Analog - M	**Green Signal Output**
BOUT	AO Analog - M	**Blue Signal Output**

Power and Ground Signals

Name	Tolerance	Power Plane	Type Attribute
A1XAVDD	3.3V	MAIN	Analog
A1XAVSS	0V	GROUND	Analog
A4XAVDD	3.3V	MAIN	Analog
A4XAVSS	0V	GROUND	Analog
AGPVSSREF	0V	GROUND	Analog
AUX1.8	1.8V	AUX	Digital
AUX3.3	3.3V	AUX	Digital
C1XAVDD	3.3V	MAIN	Analog
C1XAVSS	0V	GROUND	Analog

Power and Ground Signals continue

Name	Tolerance	Power Plane	Type Attribute
C4XAVDD	3.3V	MAIN	Analog
C4XAVSS	0V	GROUND	Analog
DACAVDD1	1.8V	MAIN	Analog
DACAVDD2	1.8V	MAIN	Analog
DACAVSS1	0V	GROUND	Analog
DACAVSS2	0V	GROUND	Digital
DCLKAVDD	3.3V	MAIN	Digital
DCLKAVSS	0V	GROUND	Analog
DDRAVDD	3.3V	MAIN	Analog
DDRAVSS	0V	GROUND	Analog
ECLKAVDD	3.3	MAIN	Analog
ECLKAVSS	0V	GROUND	Analog
IVDD	1.8V	MAIN	Digital
OVDD	3.3V	MAIN	Digital
PVDD	3.3V	MAIN	Digital
PVDDM	3.3V	AUX	Digital
PVDDP	1.8V	MAIN	Digital
PVDDZ	1.8V	MAIN	Digital
SDAVDD	3.3V	MAIN	Analog
SDAVSS	0V	GROUND	Analog
VDDM	2.5/3.3V	MAIN(AUX)	Digital
VDDQ	1.5/1.8/3.3V	MAIN	Digitalv
VDDZ	1.8V	MAIN	Digital
VDDMCMP	1.8V	MAIN	Analog
VTT	1.2~1.85V	MAIN	Digital
Z1XAVDD	3.3V	MAIN	Analog
Z1XAVSS	0V	GROUND	Analog
Z4XAVDD	3.3V	MAIN	Analog
Z4XAVSS	0V	GROUND	Analog

5.2 SiS650 IGUI Host/Memory Controller

Test Mode/Hardware Trap/Power Management

Name	Pin Attr	Signal Description
DLLEN#	I/O 3.3V/5V - M	**Hardware Trap pin (refer to section 5)**
DRAM_SEL	I 3.3V/5V - AUX	**Hardware Trap pin (refer to section 5)**
TRAP[1:0]	I 3.3V/5V - M	**Hardware Trap pins (refer to section 5)**
ENTEST	I 3.3V/5V - M	**Test Mode enable pin**
TESTMODE[2:0]	I 3.3V/5V - M	**Test Mode select pin** **Nand Tree Test: 100**
AUXOK	I 3.3V - AUXI	**Auxiliary Power OK :** This signal is supplied from the power source of resume well. It is also used to reset the logic in resume power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
PCIRST#	I 3.3V - AUXI	**PCI Bus Reset :** PCIRST# is supplied from SiS MuTIOL Media IO SiS961.
PWROK	I 3.3V - AUXI	**Main Power OK :** A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, CPURST and PCIRST# will all be asserted until after PWROK goes high for 24 ms.

5.3 SiS961 MuTIOL Media I/O Controller

Host Bus Interface

Name	Pin Attr	Signal Description
FERR#	I 1.1V/2.65V -M	**Floating Point Error:** CPU will assert this signal upon a floating point error occurring.
IGNNE#	OD 1.1V/2.65V -M	**Ignore Numeric Error:** IGNNE# is asserted to inform CPU to ignore a numeric error.
NMI	OD 1.1V/2.65V -M	**Non-Maskable Interrupt:** A rising edge on NMI will trigger a non-maskable interrupt to CPU.
INTR	OD 1.1V/2.65V -M	**Interrupt Request:** High-level voltage of this signal conveys to CPU that there is outstanding interrupt(s) needed to be serviced.
APICD[1:0]	I/OD 1.1V/2.65V -M	**APIC Data:** These two signals are used to send and receive APIC data.
CPUSLP#/ CPUSTP#	OD 1.1V/2.65V -M	**CPU Sleep:** The CPUSLP# can be used to force CPU enter the Sleep state. **CPU Clock STOP:** For Intel Mobile processor, this signal can be used to stop the clock to the processor. If the processor is in Quick Start state and the processor clock is stopped, the processor will enter the Deep Sleep state. For AMD processor, this signal can be to reduce processor voltage during C3/S1 state.
STPCLK#	OD 1.1V/2.65V -M	**Stop Clock:** STPCLK# will be asserted to inhibit or throttle CPU activities upon a pre-defined power management event occurs
INIT#	OD 1.1V/2.65V -M	**Initialization:** INIT is used to re-start the CPU without flushing its internal caches and registers. In Pentium III platform it is active high. This signal requires an external pull-up resistor tied to 3.3V.
APICCK	I 2.5V - M	**APIC Clock:** This signal is used to determine when valid data is being sent over the APCI bus.
A20M#	OD 1.1V/2.65V- M	**Address 20 Mask:** When A20M# is asserted, the CPU A20 signal will be forced to “0”

MuTIOL Connect Interface

Name	Pin Attr	Signal Description
ZCLK	I 3.3V - M	**Megaband I/O Connect Clock**
ZUREQ	I/O 1.8V - M	**Megaband I/O Conect Controll pins**
ZDREQ	I/O 1.8V - M	**Megaband I/O Conect Controll pins**
ZSTB[1:0]	I/O 1.8V - M	**Megaband I/O Connect Strobe**
ZSTB[1:0]#	I/O 1.8V - M	**Strobe Compliment**
ZAD[15:0]	I/O 1.8V - M	**Address/Data pins**
ZVRE	I -M	**Megaband I/O Connect I/O reference voltage**
ZCMP_N	I -M	**N-MOS Compensation Input**
ZCMP_P	I -M	**P-MOS Compensation input**

PCI Interface Continue

Name	Pin Attr	Signal Description
PCICLK	I 3.3V/5V -M	**PCI Clock:** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS961. It runs at the same frequency and skew of the PCI local bus.
C/BE[3:0]#	I/O 3.3V/5V -M	**PCI Bus Command and Byte Enables:** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS961 is a PCI bus master and inputs when it is a PCI slave.
PLOCK#	I/O 3.3V/5V -M	**PCI Lock:** When PLOCK# is sampled asserted at the beginning of a PCI cycle, SiS961 considers itself being locked and remains in the locked state until PLOCK# is sampled and negated at the following PCI cycle.

5.3 SiS961 MuTIOL Media I/O Controller

PCI Interface Continue

Name	Pin Attr	Signal Description
AD[31:0]	I/O 3.3V/5V -M	**PCI Address /Data Bus:** In address phase: 1.When the SiS961 is a PCI bus master, AD[31:0] are output signals. 2.When the SiS961 is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS961 is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS961 is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
PAR	I/O 3.3V/5V -M	**Parity:** SiS961 drives out Even Parity covering AD[31:0] and C/BE[3:0]#. It does not check the input parity signal.
FRAME#	I/O 3.3V/5V -M	**Frame#:** FRAME# is an output when the SiS961 is a PCI bus master. The SiS961 drives FRAME# to indicate the beginning and duration of an access. When the SiS961 is a PCI slave device, FRAME# is an input signal.
IRDY#	I/O 3.3V/5V -M	**Initiator Ready:** IRDY# is an output when the SiS961 is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS961 is a PCI slave, IRDY# is an input pin.
TRDY#	I/O 3.3V/5V -M	**Target Ready:** TRDY# is an output when the SiS961 is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS961 is a PCI master, it is an input pin.
STOP#	I/O 3.3V/5V -M	**Stop#:** STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnection, retry, and target-abortion sequences on the PCI bus.

PCI Interface

Name	Pin Attr	Signal Description
DEVSEL#	I/O 3.3V/5V -M	**Device Select:** As a PCI target, SiS961 asserts DEVSEL# by doing positive or subtractive decoding. SiS961 positively asserts DEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS961 is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PREQ[4:0]#	I 3.3V/5V -M	**PCI Bus Request:** PCI Bus Master Request Signals
PGNT[4:0]#	O 3.3V –M	**PCI Bus Grant:** PCI Bus Master Grant Signals
PREQ5# / GPIO5	I I/O 3.3V/5V- M	**PCI Bus Request:** PCI Bus Master Request Signal
PGNT5# / GPIO6	O I/O 3.3V- M	**PCI Bus Grant:** PCI Bus Master Grant Signal
INT[A:D]#	I 3.3V/5V –M	**PCI interrupt A,B,C,D:** The PCI interrupts will be connected to the inputs of the internal Interrupt controller through the rerouting logic associated with each PCI interrupt.
PCIRST#	O 3.3V –M	**PCI Bus Reset:** PCIRST# will be asserted during the period when PWROK is low, and will be kept on asserting until about 24ms after PWROK goes high.
SERR#	I 3.3V/5V –M	**System Error:** When sampled active low, a non-maskable interrupt (NMI) can be generated to CPU if enabled.

5.3 SiS961 MuTIOL Media I/O Controller

IED Interface

Name	Pin Attr	Signal Description
IDA[15:0]	I/O 3.3V/5V -M	Primary Channel Data Bus
IDB[15:0]	I/O 3.3V/5V -M	Secondary Channel Data Bus
IDECSA[1:0]#	O 3.3V -M	Primary Channel CS[1:0]
IDECSB[1:0]#	O 3.3V -M	Secondary Channel CS[1:0]
IIOR[A:B]#	O 3.3V -M	Primary/Secondary Channel IOR# Signals
IIOW[A:B]#	O 3.3V -M	Primary/Secondary Channel IOW# Signals
ICHRDY[A:B]	I 3.3V/5V -M	Primary/Secondary Channel ICHRDY# Signals
IDREQ[A:B]	I 3.3V/5V -M	Primary/Secondary Channel DMA Request Signals
IDACK[A:B]#	O 3.3V -M	Primary/Secondary Channel DMACK# Signals
IIRQ[A:B]	I 3.3V/5V -M	Primary/Secondary Channel Interrupt Signals
IDSAA[2:0]	O 3.3V -M	Primary Channel Address [2:0]
IDSAB[2:0]	O 3.3V -M	Secondary Channel Address [2:0]
CBLID[A:B]	I 3.3V/5V -M	Primary/Secondary Ultra-66 Cable ID

Legacy I/O and Miscellaneous Signals

Signal Name	Pin Attr	Signal Description
SPK	O 3.3V -M	**Speaker output:** The SPK is connected to the system speaker.
ENTEST	I 3.3V/5V -M	SiS961 Test Mode Enable Pin
OSCI	I 3.3V -M	SiS961 Test Mode Enable Pin

Power Management Interface

Name	Pin Attr	Signal Description
ACPILED	OD <=5V -AUX	**ACPILED :** ACPILED can be used to control the blinking of an LED at the frequency of 1Hz to indicate the system is at power saving mode.
EXTSMI# / GPIO3	I I/O 3.3V/5V -M	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI# event to the ACPI compatible power management unit.
PME#	I 3.3V/5V -AUX	**PME# :** When the system is in power-down mode, an active low event on PME# will cause the PSON# to go low and hence turn on the power supply. When the system is in suspend mode, an active PME# event will cause the system wakeup and generate an SCI/SMI#.
PSON#	OD <=5V -AUX	**ATX Power ON/OFF control:** PSON# is used to control the on/off state of the ATX power supply. When the ATX power supply is in the OFF state, an activated power-on event will force the power supply to ON state.
AUXOK	I 3.3V -AUX	**Auxiliary Power OK:** This signal is supplied from the AUX power source. It is also used to reset the logic in AUX power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
PWRBTN#	I 3.3V/5V -AUX	**Power Button:** This signal is from the power button switch and will be monitored by the ACPI-compatible power management unit to switch the system between working and sleeping states.
RING / GPIO8	I I/O 3.3V/5V -AUX	**Ring Indication:** An active RING pulse and lasting for more than 4ms will cause a wakeup event for system to wake from S1~S5.
BCLK_STP# GPIO12	O I/O 3.3V/5V -AUX	**Stop CPU clock:** Output to the external clock generator for it to turn off the CPU clock during C3/Sx.
DPRSLPVR GPIO13	O O 3.3V/5V -AUX	**Deeper Sleep:** DPRSLP# can be used to lower the Intel processor voltage during C3/S1 state.

5.3 SiS961 MuTIOL Media I/O Controller

LPC Interface

Name	Pin Attr	Signal Description
LAD[3:0]	I/O 3.3V/5V-M	**LPC Address/Data Bus:** LPC controller drives these four pins to transmit LPC command, address, and data to LPC device.
LDRQ#	I 3.3V/5V-M	**LPC DMA Request 0:** This pin is used by LPC device to request DMA cycle.
LDRQ1# / GPIO1	I I/O 3.3V/5V-M	**LPC DMA Request 1:** This pin is used by LPC device to request DMA cycle.
LFRAME#	O 3.3V -M	**LPC Frame:** This pin is used to notify LPC device that a start or a abort LPC cycle will occur.
SIRQ	I/O 3.3V/5V -M	I/O 3.3V/5V -M

AC'97 Interface

Name	Pin Attr	Signal Description
AC_BIT_CLK	I 3.3V/5V -M	**AC'97 Bit Clock:** This signal is a 12.288MHz serial data clock, which is generated by primary Codec.
AC_RESET#	O 3.3V -AUX	**AC'97 Reset:** Hardware reset signal for external Codecs.
AC_SDIN0	I 3.3V/5V -AUX	**AC'97 Serial Data Input :** Serial data input from primary Codec.
AC_SDIN1	I 3.3V/5V -AUX	**AC'97 Serial Data Input:** Serial data input from secondary Codec. When Modem Codec is used, this pin dedicate to Modem Serial data input.
AC_SDIN[3:2]/ GPIO[10:9]	I I/O 3.3V/5V -AUX	**AC'97 Serial Data Input:** Serial data input from third and forth Audio Codec.
AC_SDOUT	O 3.3V -M	**AC'97 Serial Data Output:** Serial data output to Codecs.
AC_SYNC	O 3.3V -M	**AC'97 Synchronization:** This is a 48KHz signal, which is used to synchronize the Codecs

TRC Interface

Name	Pin Attr	Signal Description
BATOK	I 3.3V -RTC	**Battery Power OK:** When the internal RTC is enabled, this signal is used to indicate that the power of RTC well is stable. It is also used to reset the logic in RTC well. If the internal RTC is disabled, this pin should be tied low.
OSC32KHI	I 3.3V-RTC	**RTC 32.768 KHz Input:** When internal RTC is enabled, this pin provides the 32.768 KHz clock signal from external crystal or oscillator.
OSC32KHO	O <3.3V -RTC	**RTC 32.768 KHz Output:** When internal RTC is enabled, this pin should be connected with the other end of the 32.768 KHz crystal or left unconnected if an external oscillator is used.
PWROK	I 3.3V-RTC	**Main Power OK**: A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, PCIRST# will all be asserted until after PWROK goes high for 12 ms.

USB Interface

Name	Pin Attr	Signal Description
USBCLK48M	I 3.3V/5V -M	**USB 48 MHz clock input:** This signal provides the fundamental clock for the USB Controller.
OC[0:5]#	I/O 3.3V/5V - AUX	**USB Port 0-5 Overcurrent Detection:** OC[0:5]# are used to detect the overcurrent condition of USB Ports 0-5.
UV[2:0]+, UV[2:0]-	I/O 3.3V - AUX	**USB Port** [**2:0**] **Differential**: These differential pairs are used to transmit Data/Address /Command signals for ports 0-2. (USB controller 1)
UV[5:3]+, UV[5:3]-	I/O 3.3V - AUX	**USB Port [5:3] Differential**: These differential pairs are used to transmit Data/Address/ Command signals for ports 3-5. (USB controller 2)

5.3 SiS961 MuTIOL Media I/O Controller

Keyboard Control Interface

Name	Pin Attr	Signal Description
KBDAT / GPIO15	I/OD O/OD 3.3V/5V -AUX	**Keyboard Dada:** When the internal keyboard controller is enabled, this pin is used as the keyboard data signal.
KBCLK / GPIO16	I/OD O/OD 3.3V/5V -AUX	**Keyboard Clock:** When the internal keyboard controller is enabled, this pin is used as the keyboard clock signal.
PMDAT / GPIO17	I/OD O/OD 3.3V/5V -AUX	**PS2 Mouse Data:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as PS2 mouse data signal.
PMCLK / GPIO18	I/OD O/OD 3.3V/5V -AUX	**PS2 Mouse Clock:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as the PS2 mouse clock signal.

MAC Interface Continue

Name	Pin Attr	Signal Description
RXER	I 3.3V/5V -AUX	**RX Packet Error** This event is signaled after the last received descriptor in a failed packet reception that has been updated with valid status.
MIICLK25M	I 3.3V/5V -AUX	**PHY 25MHz Clock Input:** This pin provides the 25MHz clock signal input to the built-in oscillator.
MDC	O 3.3V -AUX	**Management Data Clock:** Clock signal with a maximum rate of 2.5MHz used to transfer management data for the external physical unit on the MIIMDIO pin.
TXD[0:3]	I 3.3V/5V -AUX	**Receive Data:** This is a group of 4 data signals aligned on nibble boundaries which are driven synchronous to the RXCLK by the external physical unit.
TXEN	O 3.3V -AUX	**Transmit Data:** This is a group of 4 data signals which are driven synchronous to the TXCLK for transmission to the external physical unit.
RXD[0:3]	I 3.3V/5V -AUX	**Receive Data:** This is a group of 4 data signals aligned on nibble boundaries which are driven synchronous to the RXCLK by the external physical unit.

MAC Interface

Name	Pin Attr	Signal Description
TXEN	O 3.3V -AUX	**Transmit Enable:** When set to a 1, and the transmit state machine is idle, then the transmit state machine becomes active. This bit will read back as a 1 whenever the transmit state machine is active. After initial power-up, software must insure that the transmitter has completely reset before setting this bit
MDIO	I/O 3.3V/5V -AUX	**Management Data I/O:** Bi-direction signal used to transfer management information for the external physical unit. Requires external pull-up resistor.
RXDV	I 3.3V/5V -AUX	**Receive Data Valid**. This indicates that the external physical unit is presenting recovered and decoded nibbles on the RXD[3:0] and that RXCLK is synchronous to the recovered data. This signal will encompass the frame, starting with the Start-Of-Frame delimiter and excluding the End-Of-Frame delimiter.
COL	I 3.3V/5V -AUX	**Collision Detect:** This signal is asserted high asynchronous by the external physical unit upon detection of a collision on the medium. It'll remain asserted as long as the collision condition persists.
CRS	I 3.3V/5V -AUX	**Carrier Sense:** This signal is asserted high asynchronously by the physical unit upon detection of a non-idle medium.
RXCLK	I 3.3V/5V -AUX	**Receive Clock** A continuous clock that is recovered from the incoming data. During 100Mb/s operation RXCLK is 25MHz and during 10Mb/s this is 2.5MHz.
TXCLK	I 3.3V/5V -AUX	**Transmit Clock** A continuous clock that is sourced by the physical unit. During 100Mb/s operation RXCLK is 25MHz and during 10Mb/s this is 2.5MHz.

5.3 SiS961 MuTIOL Media I/O Controller

Power and Ground Signals

Name	Tolerance	Power Plane	Type Attribute
VSS	0V	GROUND	Digital
VSSZ	0V	GROUND	Digital
IVDD	1.8V	MAIN	Digital
PVDDZ	1.8V	MAIN	Digital
VDDZ	1.8V	MAIN	Digital
VDDZCMP	1.8V	MAIN	Analog
VSSZCMP	0V	GROUND	Analog
ZVSSREF	0V	GROUND	Analog
PVDD	3.3V	MAIN	Digital
OVDD	3.3V	MAIN	Digital
VTT	1.1V-2.65V	MAIN	Digital
IVDD_AUX	1.8V	AUX	Digital
PVDD_AUX	3.3V	AUX	Digital
OVDD_AUX	3.3V	AUX	Digital
MIIAVDD	3.3V	AUX	Analog
MIIAVSS	0V	GROUND	Analog
USBVDD	3.3V	AUX	Analog
USBVSS	0V	GROUND	Analog
RTCVDD	3.3V	RTC	Analog
RTCVSS	0V	GROUND	Analog
Z1XAVDD	3.3V	MAIN	Analog
Z1XAVSS	0V	GROUND	Analog
Z4XAVDD	3.3V	MAIN	Analog
Z4XAVSS	0V	GROUND	Analog
IDEAVDD	1.8V	MAIN	Analog
IDEAVSS	0V	GROUND	Analog

General Purpose I/O

Signal Name	Pin Attr	Signal Description
GPIO[6:0]	I/O 3.3V/5V -M	**GPIO:** Can be a general purpose input or output.
GPIO14,[12:7]	I/O 3.3V/5V -AUX	**GPIO :** Can be a general purpose input or output.
GPIO13	O 3.3V/5V - AUX	**GPO:** Can be a general purpose output.
GPIO[18:15]	O 3.3V/5V - AUX	**GPO:** Can be a general purpose output.
GPIO[20:19]	I/O 3.3V/5V - AUX	**GPIO:** Can be a general purpose input or output.

5.4 SiS301LV / Chrontel CH7019 TV/LVDS Encoder

Pin #	Type	Symbol	Description
66,101	In/Out	**H1,H2**	**Horizontal Sync Input / Output** When the SYO control bit is low, these pins accept a horizontal sync inputs for use with the input data. The amplitude will be 0 to VDDV. VREF1 is the threshold level for these inputs. These pins must be used as inputs in RGB Bypass mode. When the SYO control bit is high, the TV encoder will output a horizontal sync pulse 64 pixels wide to one of these pins. The output is driven from the DVDD supply. This output is valid only when TV-Out is in operation.
65,102	In/Out	**V1,V2**	**Vertical Sync Input / Output** When the SYO control bit is low, these pins accept a vertical sync inputs for use with the input data. The amplitude will be 0 to VDDV. VREF1 signal is the threshold level. These pins must be used as inputs in RGB Bypass mode. When the SYO control bit is high, the TV encoder will output a vertical sync pulse one line wide to one of these pins. The output is driven from the DVDD supply. This output is valid only when TV-Out is in operation.
63,104	In	**DE1,DE2**	**Data Enable** These pins accept a data enable signal which is high when active video data is input to the device, and remains low during all other times. The levels are 0 to VDDV. VREF1 is the threshold level. One of these inputs is used by the LVDS links. The TV-Out function uses H and V sync signals and values in the SAV register as reference to active video.
62,105	Out	**FLD/STL1** **FLD/STL2**	**TV Field / Flat Panel Stall Signal** These outputs can be programmed to be either a TV Field output from the TV encoder or a Stall output from the flat panel Up-scaler. These outputs are tri-stated upon power up.
107	In/Out	**SPD**	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port, and uses VREF2 / 2 as the threshold voltage. VREF2 divide by 2 function is generated on-chip.
108	In	**SPC**	**Serial Port Clock Input** This pin functions as the clock input of the serial port and uses VREF2 / 2 as the threshold voltage. VREF2 divide by 2 function is generated on-chip.
106	In	**AS**	**Address Select** (Internal Pull-up) This pin determines the device address of the serial port.

Pin #	Type	Symbol	Description
112	In/Out	**SDD**	**Low-Voltage DDC Serial Data** Low-voltage serial data for DDC. It uses VREF2 / 2 as the threshold voltage. VREF2 divide by 2 function is generated on-chip.
113	In/Out	**SDC**	**Low-Voltage DDC Serial Clock** Low-voltage serial clock for DDC. It uses VREF2 / 2 as the threshold voltage. VREF2 divide by 2 function is generated on-chip.
114,116	In/Out	**DD1, DD2**	**DDC Serial Data** Serial data for DDC. (0V to 5V) .
111	In	**VREF2**	**Reference Voltage 2** Used to generate the threshold level for SDD, SDC, SPD and SPC port. This pin should be tied externally to the maximum voltage seen by the ports. (1.5V to 3.3V).
115,117	In/Out	**DC1,DC2**	**DDC Serial Clock** Clock for DDC. (0V to 5V)
123-126 56,57	In/Out	**GPIO[5:0]**	**General Purpose Input / Output [5:0]** These pins provide general purpose I/O and are controlled via the serial port. (3.3V).
127	Out	**ENAVDD**	**Panel Power Enable** Enable panel VDD. (3.3V)
128	Out	**ENABLK**	**Back Light Enable** Enable Back-Light of LCD Panel. (3.3V)
121	In	**HPD**	**Hot Plug Detect** (Internal Pull-down) This input pin determines whether a CRT monitor is connected to the VGA connector. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the HPINT* pin pulling low.
122	Out	**HPINT***	**Hot Plug Interrupt Output** This pin provides an open drain output, which pulls low when a termination change has been detected on the HPD input.
36	In	**VSWING**	**LVDS Voltage Swing Control** This pin sets the swing level of the LVDS outputs. A 2.4K Ohm resistor should be connected between this pin and LGND (pin 35) using short and wide traces.
58	In	**RESET***	**Reset * Input** (Internal Pull-up) When this pin is low, the device is held in the power on reset condition. When this pin is high, reset is controlled through the serial port.

5.4 SiS301LV / Chrontel CH7019 TV/LVDS Encoder

Pin #	Type	Symbol	Description
2	Analog	**LPLLCAP**	**LVDS PLL Capacitor** This pins allows coupling of any signal to the on-chip loop filter capacitor.
5,24	Out	**LL2C,LL1C**	**Positive LVDS differential Clock2 & Clock1**
6,25	Out	**LL2C*,LL1C***	**Negative LVDS differential Clock2 & Clock1**
8,11,14,17	Out	**LDC[7:4]**	**Positive LVDS differential data[7:4]**
9,12,15,18	Out	**LDC[7:4]***	**Negative LVDS differential data[7:4]**
21,27,30,33	Out	**LDC[3:0]**	**Positive LVDS differential data[3:0]**
22,28,31,34	Out	**LDC[3:0]***	**Negative LVDS differential data [3:0]**
38	Analog	**ISET**	**Current Set Resistor Input** This pin sets the DAC current. A 140-ohm resistor should be connected between this pin and DAC_GND (pin 39) using short and wide traces.
40,42,44,46	Out	**DACB[3:0]**	**DAC Output B** Video Digital-to-Analog outputs.
41,43,45,47	Out	**DACA[3:0]**	**DAC Output A** Video Digital-to-Analog outputs.
120	Out	**VOUT**	**V-Sync Output** This pin is the output of a voltage translating digital buffer and is driven from V5V.
110	In	**VIN**	**V-Sync Input** This pin is the input of a voltage translating digital buffer. Input threshold can be programmed by serial port to equal to VREF2/2 or to DVDD/2. The amplitude will be 0 to VDDV. VREF1 is the threshold level for these inputs.
119	Out	**HOUT**	**H-Sync Output** This pin is the output of a voltage translating digital buffer and is driven from V5V.
109	In	**HIN**	**H-Sync Input** This pin is the input of a voltage translating digital buffer. Input threshold can be programmed by serial port to equal to VREF2/2 or to DVDD/2.
49	Out	**C/HSYNC**	**Composite / Horizontal Sync** Provides composite sync in TV modes and horizontal sync in bypass RGB mode. This pin is driven by the DVDD supply.
50	Out	**BCO/VSYNC**	**Buffered Clock Outputs / Vertical Sync** This output pin provides buffered crystal oscillator clock output or VSYNC output in bypass RGB mode. This pin is driven by the DVDD supply.

Pin #	Type	Symbol	Description
52	In	**XI/FIN**	**Crystal Input / External Reference Input** A parallel resonant 14.31818MHz crystal (+ 20 ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI/FIN input.
53	Out	**XO**	**Crystal Output** A parallel resonance 14.31818MHz crystal (+ 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
59	Out	**P-OUT**	**Pixel Clock Output** This pin provides a pixel clock signal to the VGA controller which can be used as a reference frequency. The output is selectable between 1X and 2X of the pixel clock frequency. The output driver is driven from the VDDV supply (pin 60). This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.
61	In	**VREF1**	**Reference Voltage Input 1** The VREF1 pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.
68-73,77-82	In	**D1[11:0]**	**Data1[11] through Data1[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF1 is the threshold level.
76,74	In	**XCLK1** **XCLK1***	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H1, V1 and D1[11:0] data. If differential clocks are not available, the XCLK1* input should be connected to VREF1. The clock polarity can be selected by the MCP1 control bit.
85-90,94-99	In	**D2[11:0]**	**Data2[11] through Data2[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to DVDDV. VREF1 is the threshold level.
93,91	In	**XCLK** **XCLK2***	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H2, V2 and D2[11:0] data. If differential clocks are not available, the XCLK2* input should be connected to VREF1. The clock polarity can be selected by the MCP2 control bit.

5.4 SiS301LV / Chrontel CH7019 TV/LVDS Encoder

Pin #	Type	Symbol	Description
118	**Power**	**V5V**	**5V supply for H/VOUT** (5V)
64,83,84,103	**Power**	**DVDD**	**Digital Supply Voltage (3.3V)**
67,75,92,100	**Power**	**DGND**	**Digital Ground**
60	**Power**	**VDDV**	**I/O Supply Voltage** (1.1V to 3.3V)
55	**Power**	**TVPLL_VDD**	**TV PLL Supply Voltage** (3.3V)
54	**Power**	**TVPLL_VCC**	**TV PLL Supply Voltage** (3.3V)
51	**Power**	**TVPLL_GND**	**TV PLL Ground**
37	**Power**	**DAC_VDD**	**DAC Supply Voltage** (3.3V)
39,48	**Power**	**DAC_GND**	**DAC Ground**
7,13,19,20,26,32	**Power**	**LVDD**	**LVDS Supply Voltage** (3.3V)
4,10,16,23,29,35	**Power**	**LGND**	**LVDS Ground**
1	**Power**	**LPLL_VDD**	**LVDS PLL Supply Voltage** (3.3V)
3	**Power**	**LPLL_GND**	**LVDS PLL Ground**

5.5 PCI1410GGU PCMCIA Controller

Power Supply

Name	I/O	Description
GND		Device ground terminals
VCC		Power supply terminal for core logic (3.3V)
VCCCB		Clamp voltage for PC Card interface. Matches card signaling environment, 5 V or 3.3 V.
VCCI		Clamp voltage for interrupt subsystem interface and miscellaneous I/O, 5 V or 3.3 V
VCCP		Clamp voltage for PCI signaling, 5 V or 3.3 V

PC Card Power Switch

Name	I/O	Description
VCCD0 **VCCD1**	O	Logic controls to the TPS2211 PC Card power interface switch to control AVCC.
VPPD0 **VPPD1**	O	Logic controls to the TPS2211 PC Card power interface switch to control AVPP.

PCI System

Name	I/O	Description
GRST#	I	Global reset. When the global reset is asserted, the GRST# signal causes the PCI1410 to place all output buffers in a high-impedance state and reset all internal registers. When GRST# is asserted, the device is completely in its default state. For systems that require wake-up from D3, GRST# will normally be asserted only during initial boot. PRST# should be used following initial boot so that PME context is retained when transitioning from D3 to D0. For systems that do not require wake-up from D3, GRST# should be tied to PRST#. When the SUSPEND# mode is enabled, the device is protected from the GRST#, and the internal registers are preserved. All outputs are placed in a high-impedance state, but the contents of the registers are preserved.
PCLK	I	PCI bus clock. PCLK provides timing for all transactions on the PCI bus. All PCI signals are sampled at the rising edge of PCLK.
PRST#	I	PCI reset. When the PCI bus reset is asserted, PRST# causes the PCI1410 to place all output buffers in a high-impedance state and reset internal registers. When PRST# is asserted, the device is completely nonfunctional. After PRST is deasserted, the PCI1410 is in a default state. When the SUSPEND# mode is enabled, the device is protected from the PRST#, and the internal registers are preserved. All outputs are placed in a high-impedance state, but the contents of the registers are preserved.

PCI Interface Control

Name	I/O	Description
DEVSEL#	I/O	PCI device select. The PCI1410 asserts DEVSEL# to claim a PCI cycle as the target device. As a PCI initiator on the bus, the PCI1410 monitors DEVSEL# until a target responds. If no target responds before timeout occurs, then the PCI1410 terminates the cycle with an initiator abort.
FRAME#	I/O	PCI cycle frame. FRAME# is driven by the initiator of a bus cycle. FRAME# is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When FRAME# is deasserted, the PCI bus transaction is in the final data phase.
GNT#	I	PCI bus grant. GNT# is driven by the PCI bus arbiter to grant the PCI1410 access to the PCI bus after the current data transaction has completed. GNT# may or may not follow a PCI bus request, depending on the PCI bus parking algorithm.
IDSEL	I	Initialization device select. IDSEL selects the PCI1410 during configuration space accesses. IDSEL can be connected to one of the upper 24 PCI address lines on the PCI bus.
IRDY#	I/O	PCI initiator ready. IRDY# indicates the PCI bus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCLK where both IRDY# and TRDY# are asserted. Until IRDY# and TRDY# are both sampled asserted, wait states are inserted.
PERR#	I/O	PCI parity error indicator. PERR# is driven by a PCI device to indicate that calculated parity does not match PAR when PERR# is enabled through bit 6 of the command register.
REQ#	O	PCI bus request. REQ# is asserted by the PCI1410 to request access to the PCI bus as an initiator.
SERR#	O	PCI system error. SERR# is an output that is pulsed from the PCI1410 when enabled through bit 8 of the command register indicating a system error has occurred. The PCI1410 need not be the target of the PCI cycle to assert this signal. When SERR# is enabled in the command register, this signal also pulses, indicating that an address parity error has occurred on a CardBus interface.
STOP#	I/O	PCI cycle stop signal. STOP# is driven by a PCI target to request the initiator to stop the current PCI bus transaction. STOP# is used for target disconnects and is commonly asserted by target devices that do not support burst data transfers.
TRDY#	I/O	PCI target ready. TRDY# indicates the primary bus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCLK when both IRDY# and TRDY# are asserted. Until both IRDY# and TRDY# are asserted, wait states are inserted.

5.5 PCI1410GGU PCMCIA Controller

Multifunction and Miscellaneous Pins

Name	I/O	Description
MFUNC0	I/O	Multifunction terminal 0. MFUNC0 can be configured as parallel PCI interrupt INTA#, GPI0, GPO0, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, or a parallel IRQ.
MFUNC1	I/O	Multifunction terminal 1. MFUNC1 can be configured as GPI1, GPO1, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, or a parallel IRQ. Serial data (SDA). When VPPD0 and VPPD1 are high after a PCI reset, the MFUNC1 terminal provides the SDA signaling for the serial bus interface. The two-pin serial interface loads the subsystem identification and other register defaults from an EEPROM after a PCI reset.
MFUNC2	I/O	Multifunction terminal 2. MFUNC2 can be configured as PC/PCI DMA request, GPI2, GPO2, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, RI_OUT#, or a parallel IRQ.
MFUNC3	I/O	Multifunction terminal 3. MFUNC3 can be configured as a parallel IRQ or the serialized interrupt signal IRQSER.
MFUNC4	I/O	Multifunction terminal 4. MFUNC4 can be configured as PCI LOCK#, GPI3, GPO3, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, RI_OUT#, or a parallel IRQ. Serial clock (SCL). When VPPD0 and VPPD1 are high after a PCI reset, the MFUNC4 terminal provides the SCL signaling for the serial bus interface. The two-pin serial interface loads the subsystem identification and other register defaults from an EEPROM after a PCI reset.
MFUNC5	I/O	Multifunction terminal 5. MFUNC5 can be configured as PC/PCI DMA grant, GPI4, GPO4, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, or a parallel IRQ.
MFUNC6	I/O	Multifunction terminal 6. MFUNC6 can be configured as a PCI CLKRUN# or a parallel IRQ.
RI_OUT#/PME#	O	Ring indicate out and power management event output. Terminal provides an output for ring-indicate or PME# signals.
SPKROUT	O	Speaker output. SPKROUT is the output to the host system that can carry SPKR# or CAUDIO through the PCI1410 from the PC Card interface. SPKROUT is driven as the exclusive-OR combination of card SPKR#//CAUDIO inputs.
SUSPEND#	I	Suspend. SUSPEND# protects the internal registers from clearing when the GRST# or PRST# signal is asserted.

PCI Address and Data

Name	I/O	Description
AD[31:0]	I/O	PCI address/data bus. These signals make up the multiplexed PCI address and data bus on the primary interface. During the address phase of a primary bus PCI cycle, AD31–AD0 contain a 32-bit address or other destination information. During the data phase, AD31–AD0 contain data.
C/BE#[3:0]	I/O	PCI bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During the address phase of a primary bus PCI cycle, C/BE#3–C/BE#0 define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. C/BE#0 applies to byte 0 (AD7–AD0), C/BE#1 applies to byte 1 (AD15–AD8), C/BE2 applies to byte 2 (AD23–AD16), and C/BE#3 applies to byte 3 (AD31–AD24).
PAR	I/O	PCI bus parity. In all PCI bus read and write cycles, the PCI1410 calculates even parity across the AD31–AD0 and C/BE#3–C/BE#0 buses. As an initiator during PCI cycles, the PCI1410 outputs this parity indicator with a one-PCLK delay. As a target during PCI cycles, the calculated parity is compared to the initiator's parity indicator. A compare error results in the assertion of a parity error (PERR#).

16-Bit PC Card Address and Data (Slots A and B)

Name	I/O	Description
ADDR[25:0]	O	PC Card address. 16-bit PC Card address lines. ADDR25 is the most significant bit.
DATA[15:0]	I/O	PC Card data. 16-bit PC Card data lines. DATA15 is the most significant bit.

5.5 PCI1410GGU PCMCIA Controller

16-Bit PC Card Interface Control (Slots A and B)

Name	I/O	Description
BVD1 (STSCHG#/RI#)	I	Battery voltage detect 1. BVD1 is generated by 16-bit memory PC Cards that include batteries. BVD1 is used with BVD2 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. Status change. STSCHG# is used to alert the system to a change in the READY, write protect, or battery voltage dead condition of a 16-bit I/O PC Card. Ring indicate. RI is used by 16-bit modem cards to indicate a ring detection.
BVD2 (SPKR#)	I	Battery voltage detect 2. BVD2 is generated by 16-bit memory PC Cards that include batteries. BVD2 is used with BVD1 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. Speaker. SPKR# is an optional binary audio signal available only when the card and socket have been configured for the 16-bit I/O interface. The audio signals from cards A and B are combined by the PCI1410 and are output on SPKROUT. DMA request. BVD2 can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. The PC Card asserts BVD2 to indicate a request for a DMA operation.
CD1# CD2#	I	Card detect 1 and Card detect 2. CD1# and CD2# are internally connected to ground on the PC Card. When a PC Card is inserted into a socket, CD1# and CD2# are pulled low.
CE1# CE2#	O	Card enable 1 and card enable 2. CE1# and CE2# enable even- and odd-numbered address bytes. CE1# enables even-numbered address bytes, and CE2# enables odd-numbered address bytes.
INPACK#	I	Input acknowledge. INPACK# is asserted by the PC Card when it can respond to an I/O read cycle at the current address. DMA request. INPACK# can be used as the DMA request signal during DMA operations from a 16-bit PC Card that supports DMA. If it is used as a strobe, then the PC Card asserts this signal to indicate a request for a DMA operation.
IORD#	O	I/O read. IORD# is asserted by the PCI1410 to enable 16-bit I/O PC Card data output during host I/O read cycles. DMA write. IORD# is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI1410 asserts IORD# during DMA transfers from the PC Card to host memory.
IOWR#	O	I/O write. IOWR# is driven low by the PCI1410 to strobe write data into 16-bit I/O PC Cards during host I/O write cycles. DMA read. IOWR# is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI1410 asserts IOWR# during transfers from host memory to the PC Card.
OE#	O	Output enable. OE# is driven low by the PCI1410 to enable 16-bit memory PC Card data output during host memory read cycles. DMA terminal count. OE# is used as terminal count (TC) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1410 asserts OE# to indicate TC for a DMA write operation.
READY (IREQ#)	I	Ready. The ready function is provided by READY when the 16-bit PC Card and the host socket are configured for the memory-only interface. READY is driven low by the 16-bit memory PC Cards to indicate that the memory card circuits are busy processing a previous write command. READY is driven high when the 16-bit memory PC Card is ready to accept a new data transfer command. Interrupt request. IREQ# is asserted by a 16-bit I/O PC Card to indicate to the host that a device on the 16-bit I /O PC Card requires service by the host software. IREQ# is high (deasserted) when no interrupt is requested.
REG#	O	Attribute memory select. REG# remains high for all common memory accesses. When REG# is asserted, access is limited to attribute memory (OE# or WE# active) and to the I/O space (IORD# or IOWR# active). Attribute memory is a separately accessed section of card memory and is generally used to record card capacity and other configuration and attribute information. DMA acknowledge. REG# is used as a DMA acknowledge (DACK#) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1410 asserts REG to indicate a DMA operation. REG# is used in conjunction with the DMA read (IOWR#) or DMA write (IORD#) strobes to transfer data.
RESET	O	PC Card reset. RESET forces a hard reset to a 16-bit PC Card.
WAIT#	I	Bus cycle wait. WAIT# is driven by a 16-bit PC Card to extend the completion of the memory or I/O cycle in progress.
WE#	O	Write enable. WE# is used to strobe memory write data into 16-bit memory PC Cards. WE# is also used for memory PC Cards that employ programmable memory technologies. DMA terminal count. WE# is used as TC# during DMA operations to a 16-bit PC Card that supports DMA. The PCI1410 asserts WE# to indicate TC# for a DMA read operation.
WP (IOIS16#)	I	Write protect. WP applies to 16-bit memory PC Cards. WP reflects the status of the write-protect switch on 16-bit memory PC Cards. For 16-bit I/O cards, WP is used for the 16-bit port (IOIS16#) function. I/O is 16 bits. IOIS16# applies to 16-bit I/O PC Cards. IOIS16# is asserted by the 16-bit PC Card when the address on the bus corresponds to an address to which the 16-bit PC Card responds, and the I/O port that is addressed is capable of 16-bit accesses. DMA request. WP can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. If used, then the PC Card asserts WP to indicate a request for a DMA operation.
VS1# VS2#	I/O	Voltage sense 1 and voltage sense 2. VS1# and VS2#, when used in conjunction with each other, determine the operating voltage of the PC Card.

5.5 PCI1410GGU PCMCIA Controller

CardBus PC Card Interface System (Slots A and B)

Name	I/O	Description
CCLK	O	CardBus clock. CCLK provides synchronous timing for all transactions on the CardBus interface. All signals except CRST#, CCLKRUN#, CINT#, CSTSCHG, CAUDIO, CCD2#, CCD1#, CVS2, and CVS1 are sampled on the rising edge of CCLK, and all timing parameters are defined with the rising edge of this signal. CCLK operates at the PCI bus clock frequency, but it can be stopped in the low state or slowed down for power savings.
CCLKRUN#	I/O	CardBus clock run. CCLKRUN# is used by a CardBus PC Card to request an increase in the CCLK frequency, and by the PCI1410 to indicate that the CCLK frequency is going to be decreased.
CRST#	O	CardBus reset. CRST# brings CardBus PC Card-specific registers, sequencers, and signals to a known state. When CRST# is asserted, all CardBus PC Card signals are placed in a high-impedance state, and the PCI1410 drives these signals to a valid logic level. Assertion can be asynchronous to CCLK, but deassertion must be synchronous to CCLK.

CardBus PC Card Address and Data (Slots A and B)

Name	I/O	Description
CAD[31:0]	I/O	CardBus address and data. These signals make up the multiplexed CardBus address and data bus on the CardBus interface. During the address phase of a CardBus cycle, CAD31–CAD0 contain a 32-bit address. During the data phase of a CardBus cycle, CAD31–CAD0 contain data. CAD31 is the most significant bit.
CC/BE#[3:0]	I/O	CardBus bus commands and byte enables. CC/BE#3–CC/BE#0 are multiplexed on the same CardBus terminals. During the address phase of a CardBus cycle, CC/BE#3–CC/BE#0 define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. CC/BE#0 applies to byte 0 (CAD7–CAD0), CC/BE#1 applies to byte 1 (CAD15–CAD8), CC/BE#2 applies to byte 2 (CAD23–CAD8), and CC/BE#3 applies to byte 3 (CAD31–CAD24).
CPAR	I/O	CardBus parity. In all CardBus read and write cycles, the PCI1410 calculates even parity across the CAD and CC/BE# buses. As an initiator during CardBus cycles, the PCI1410 outputs CPAR with a one-CCLK delay. As a target during CardBus cycles, the calculated parity is compared to the initiator's parity indicator; a compare error results in a parity error assertion.

CardBua PC Card Interface Control (Slots A and B)

Name	I/O	Description
CAUDIO	I	CardBus audio. CAUDIO is a digital input signal from a PC Card to the system speaker. The PCI1410 supports the binary audio mode and outputs a binary signal from the card to SPKROUT.
CBLOCK#	I/O	CardBus lock. CBLOCK# is used to gain exclusive access to a target.
CCD1# **CCD2#**	I	CardBus detect 1 and CardBus detect 2. CCD1# and CCD2# are used in conjunction with CVS1 and CVS2 to identify card insertion and interrogate cards to determine the operating voltage and card type.
CE1# **CE2#**	O	Card enable 1 and card enable 2. CE1# and CE2# enable even- and odd-numbered address bytes. CE1# enables even-numbered address bytes, and CE2# enables odd-numbered address bytes.
CDEVSEL#	I/O	CardBus device select. The PCI1410 asserts CDEVSEL# to claim a CardBus cycle as the target device. As a CardBus initiator on the bus, the PCI1410 monitors CDEVSEL# until a target responds. If no target responds before timeout occurs, then the PCI1410 terminates the cycle with an initiator abort.
CFRAME#	I/O	CardBus cycle frame. CFRAME# is driven by the initiator of a CardBus bus cycle. CFRAME# is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When CFRAME# is deasserted, the CardBus bus transaction is in the final data phase.
CGNT#	O	CardBus bus grant. CGNT# is driven by the PCI1410 to grant a CardBus PC Card access to the CardBus bus after the current data transaction has been completed.
CINT#	I	CardBus interrupt. CINT# is asserted low by a CardBus PC Card to request interrupt servicing from the host.
CIRDY#	I/O	CardBus initiator ready. CIRDY# indicates the CardBus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK when both CIRDY# and CTRDY# are asserted. Until CIRDY# and CTRDY# are both sampled asserted, wait states are inserted.

5.5 PCI1410GGU PCMCIA Controller

CardBua PC Card Interface Control (Slots A and B) (Continued)

Name	I/O	Description
CPERR#	I/O	CardBus parity error. CPERR# reports parity errors during CardBus transactions, except during special cycles. It is driven low by a target two clocks following that data when a parity error is detected.
CREQ#	I	CardBus request. CREQ# indicates to the arbiter that the CardBus PC Card desires use of the CardBus bus as an initiator.
CSERR#	I	CardBus system error. CSERR# reports address parity errors and other system errors that could lead to catastrophic results. CSERR# is driven by the card synchronous to CCLK, but deasserted by a weak pullup, and may take several CCLK periods. The PCI1410 can report CSERR# to the system by assertion of SERR# on the PCI interface.
CSTOP#	I/O	CardBus stop. CSTOP# is driven by a CardBus target to request the initiator to stop the current CardBus transaction. CSTOP# is used for target disconnects, and is commonly asserted by target devices that do not support burst data transfers.
CSTSCHG	I	CardBus status change. CSTSCHG alerts the system to a change in the card's status, and is used as a wake-up mechanism.
CTRDY#	I/O	CardBus target ready. CTRDY# indicates the CardBus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK, when both CIRDY# and CTRDY# are asserted; until this time, wait states are inserted.
CVS1 **CVS2**	I/O	CardBus voltage sense 1 and CardBus voltage sense 2. CVS1 and CVS2 are used in conjunction with CCD1# and CCD2# to identify card insertion and interrogate cards to determine the operating voltage and card type.

5.6 uPD72872 IEEE1394 Controller

PCI/Cardbus Interface Signals: (52 pins)

Name	I/O	PIN NO.	IOL	Volts(V)	Function	Block*
PAR	I/O	44	PCI/Cardbus	5/3.3	**Parity** is even parity across AD0-AD31 and CBE0-CBE3. It is an input when AD0-AD31 is an input; it is an output when AD0-AD31 is an output.	Link
AD0-AD31	I/O	9, 10, 12, 13, 15-18, 23, 24, 26-29, 32, 33, 47-50, 52, 53, 55, 56, 58,59, 62, 63, 65-68	PCI/Cardbus	5/3.3	**PCI Multiplexed Address and Data**	Link
CBE0-CBE3	I	21, 34, 45, 57	-	5/3.3	**Command/Byte Enables** are multiplexed Bus Commands & Byte enables.	Link
FRAME	I/O	35	PCI/Cardbus	5/3.3	**Frame** is asserted by the initiator to indicate the cycle beginning and is kept asserted during the burst cycle. If Cardbus mode (CARD_ON = 1), this pin should be pulled up to V_{DD}.	Link
TRDY	I/O	37	PCI/Cardbus	5/3.3	**Target Ready** indicates that the current data phase of the transaction is ready to be completed.	Link
IRDY	I/O	36	PCI/Cardbus	5/3.3	**Initiator Ready** indicates that the current bus master is ready to complete the current data phase. During a write, its assertion indicates that the initiator is driving valid data onto the data bus. During a read, its assertion indicates that the initiator is ready to accept data from the currently-addressed target.	Link
REQ	O	8	PCI/Cardbus	5/3.3	**Bus_master Request** indicates to the bus arbiter that this device wants to become a bus master.	Link
GNT	I	7	-	5/3.3	**Bus_master Grant** indicates to this device that access to the bus has been granted.	Link
IDSEL	I	22	-	5/3.3	**Initialization Device Select** is used as chip select for configuration read/write transaction during the phase of device initialization. If Cardbus mode (CARD_ON = 1), this pin should be pulled up to V_{DD}.	Link
DEVSEL	I/O	39	PCI/Cardbus	5/3.3	**Device Select** when actively driven, indicates that the driving device has decoded its address as the target of the current access.	Link
STOP	I/O	40	PCI/Cardbus	5/3.3	**PCI Stop** when actively driven, indicates that the target is requesting the current bus master to stop the transaction.	Link
PME	O	3	PCI/Cardbus	5/3.3	**PME Output** for power management enable.	Link
CLKRUN	I/O	2	PCI/Cardbus	5/3.3	**PCICLK Running** as input, to determine the status of PCLK; as output, to request starting or speeding up clock.	Link
INTA	O	4	PCI/Cardbus	5/3.3	**Interrupt** the PCI interrupt request A.	Link

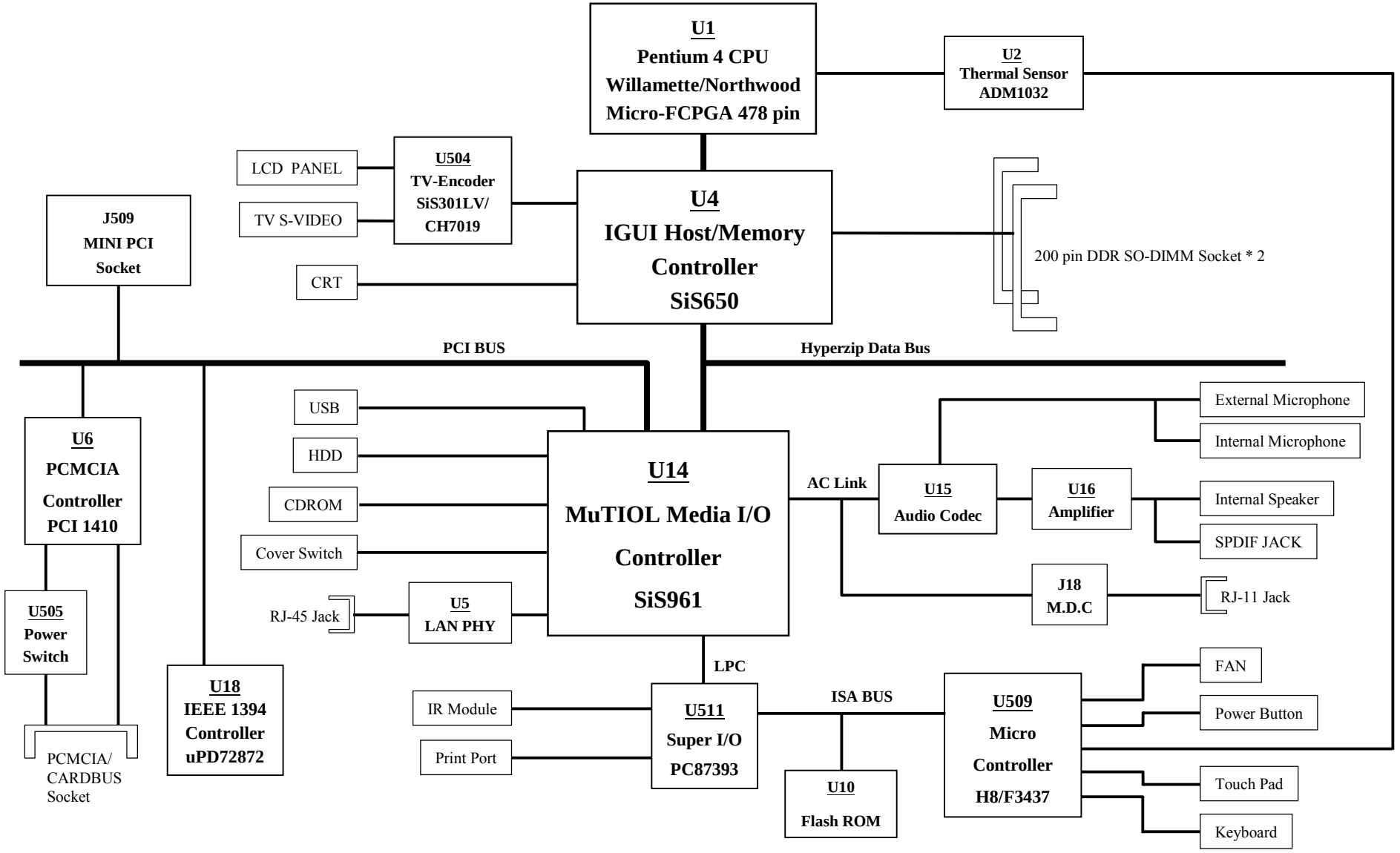
5.6 uPD72872 IEEE1394 Controller

Name	I/O	PIN NO.	IOL	Volts(V)	Function	Block*
PERR	I/O	41	PCI/Cardbus	5/3.3	**Parity Error** is used for reporting data parity errors during all PCI transactions, except a Special Cycle. It is an output when AD0-AD31 and PAR are both inputs. It is an input when AD0-AD31 and PAR are both outputs.	Link
SERR	O	42	PCI/Cardbus	5/3.3	**System Error** is used for reporting address parity errors, data parity errors during the Special Cycle, or any other system error where the effect can be catastrophic. When reporting address parity errors, it is an output.	Link
PRST	I	5	-	5/3.3	**Reset** PCI reset	Link
PCLK	I	6	-	5/3.3	**PCI Clock** 33 MHz system bus clock.	Link

Remark *: If the Link pin is pulled up, it should be connected to L_V_{DD}.

8575 N/B Maintenance

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at PIO PORT.

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Sizememory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Signon messages displayed

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code
50h	ACPI init
51h	PM init & Geyserville
52h	USB HC init

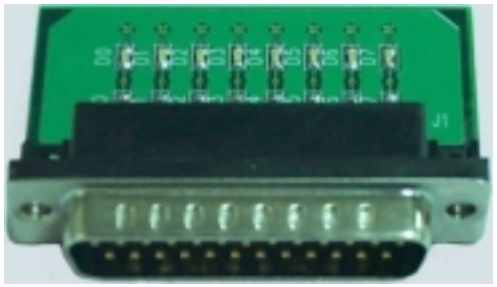
8575 N/B Maintenance

7.3 Maintenance Diagnostics

7.3.1 Diagnostic Tools :

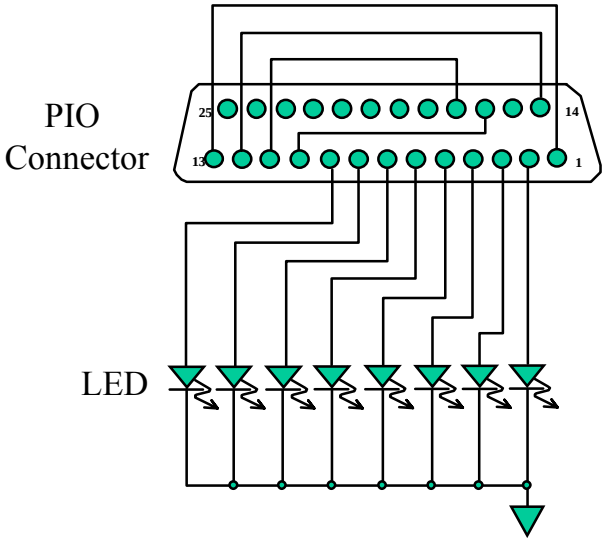
- **LED * 8**
- **PIO CONNECTOR * 1**

OR



P/N:411904800001
Description: PWA; PWA-378Port Debug BD
Note: Order it from MIC/TSSC

7.3.2 Circuit:



PIN1 : STROBE ⟷ PIN 13 : SLCT

PIN10: ACK# ⟷ PIN 16 : INT#

PIN11: BUSY ⟷ PIN 17 : SELIN#

PIN12: PTERR ⟷ PIN 14 : AUTOFD#

PIN{9:2}: PD{7:0}

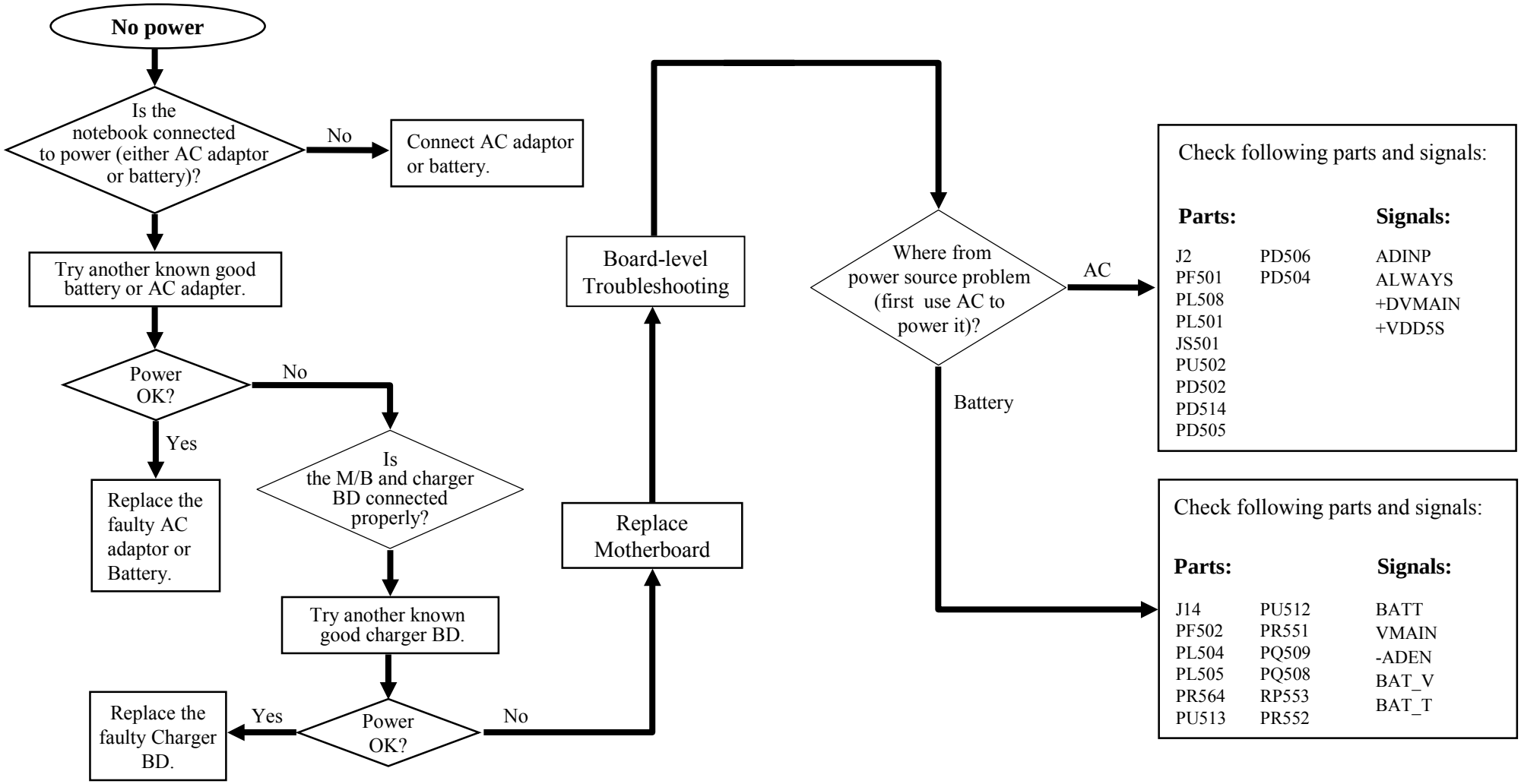
8. Trouble Shooting

- 8.1 No Power
- 8.2 No Display
- 8.3 VGA Controller Failure LCD No Display
- 8.4 External Monitor No Display
- 8.5 Memory Test Error
- 8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.7 Hard Driver Test Error
- 8.8 CD-ROM Driver Test Error
- 8.9 PIO Port Test Error
- 8.10 USB Port Test Error
- 8.11 Audio Failure
- 8.12 LAN Test Error
- 8.13 PC Card Socket Failure
- 8.14 IEEE 1394 Failure

8575 N/B Maintenance

8.1 No Power

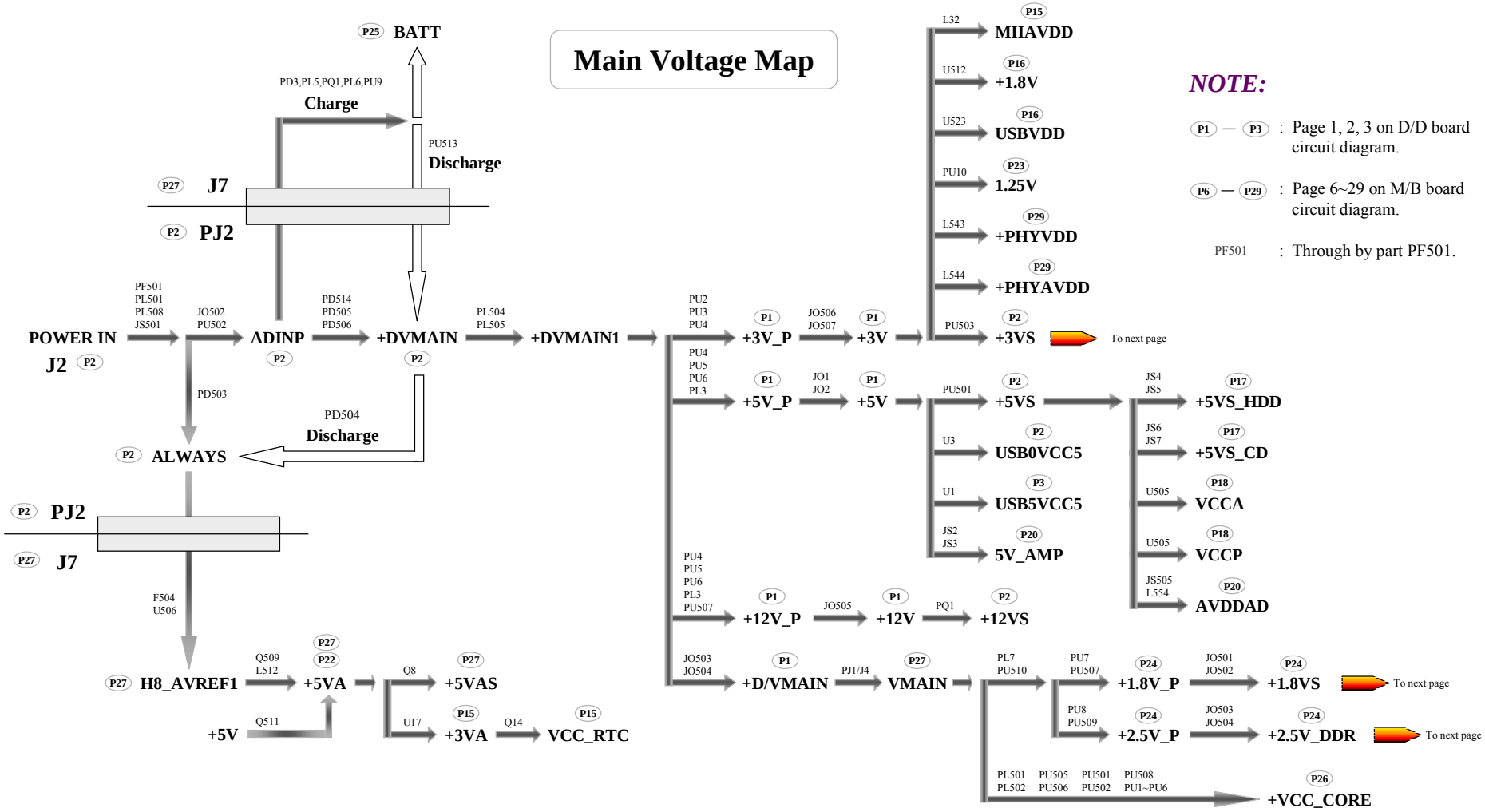
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8575 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

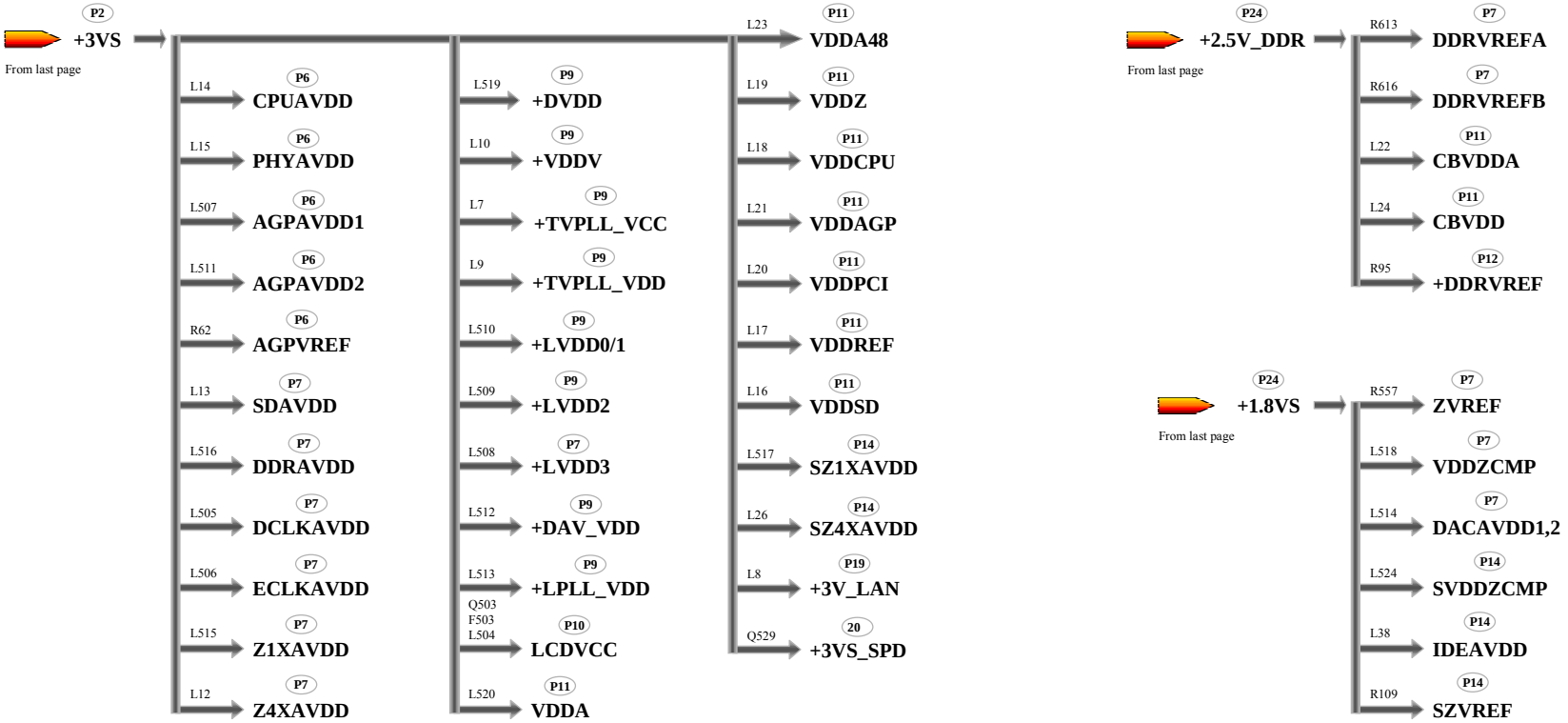


8575 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

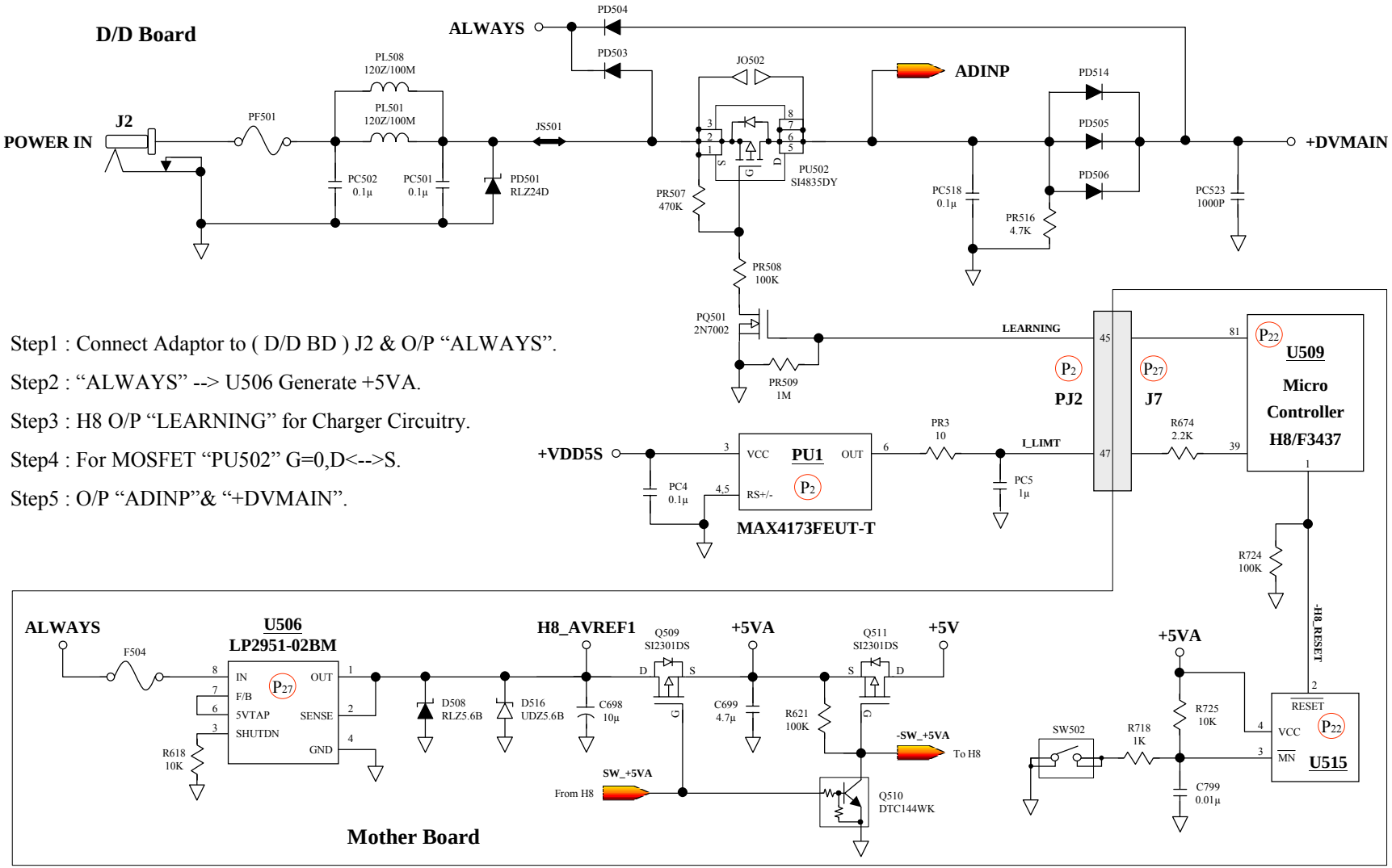
Main Voltage Map



8575 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



Step1 : Connect Adaptor to (D/D BD) J2 & O/P “ALWAYS”.

Step2 : “ALWAYS” --> U506 Generate +5VA.

Step3 : H8 O/P “LEARNING” for Charger Circuitry.

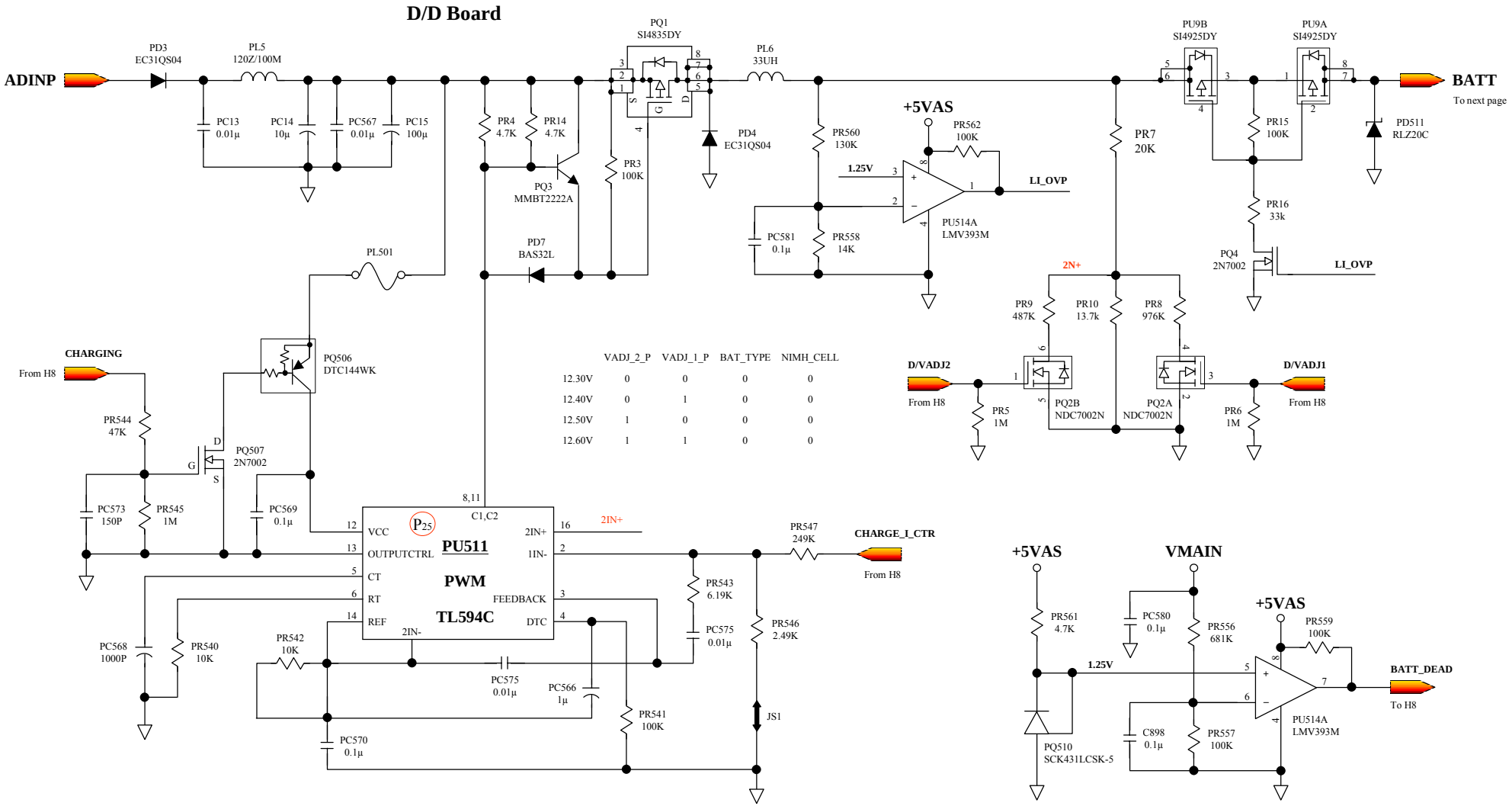
Step4 : For MOSFET “PU502” G=0,D<-->S.

Step5 : O/P “ADINP”& “+DVMAIN”.

8575 N/B Maintenance

8.1 No Power – Battery Charge

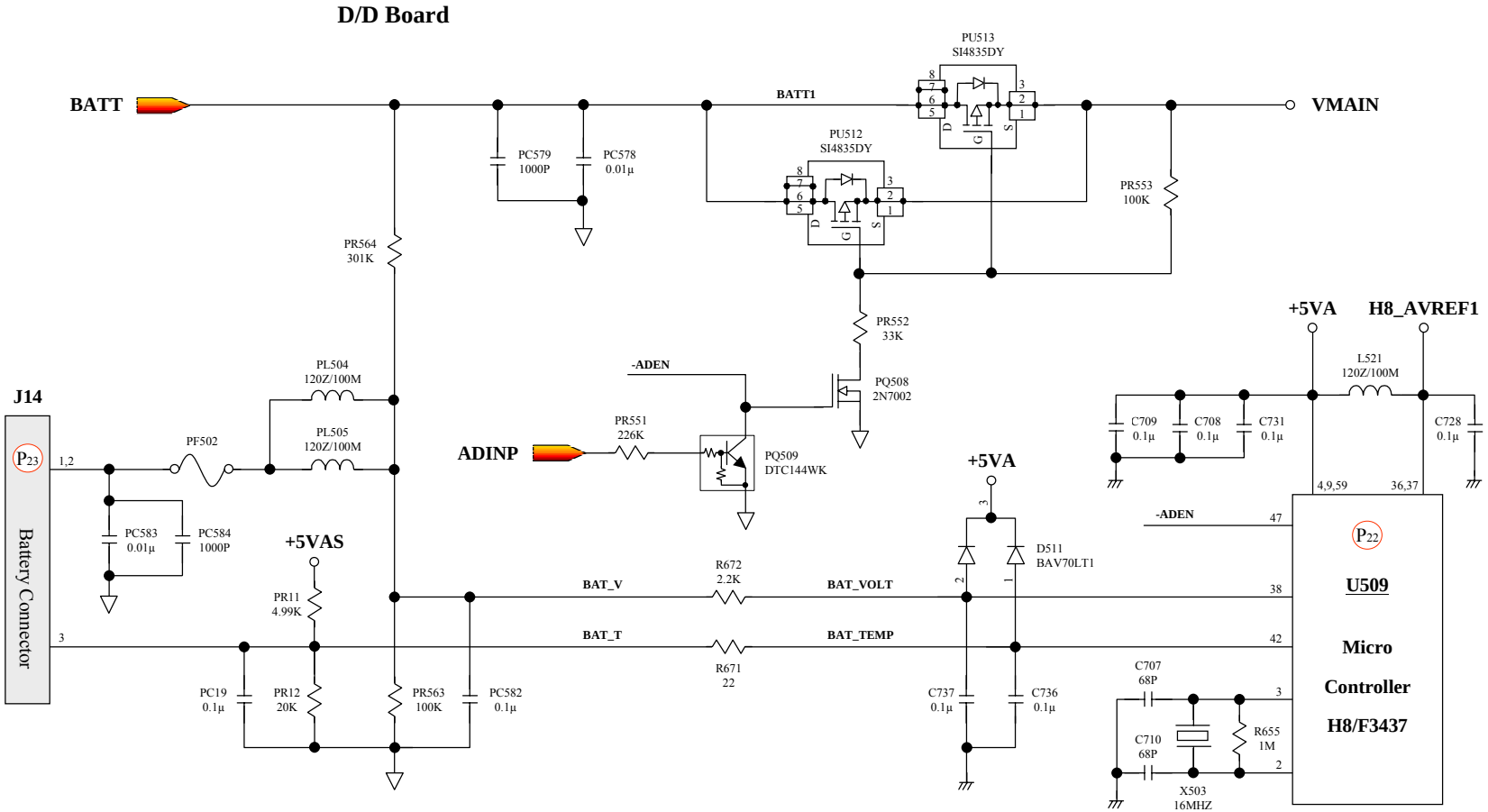
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8575 N/B Maintenance

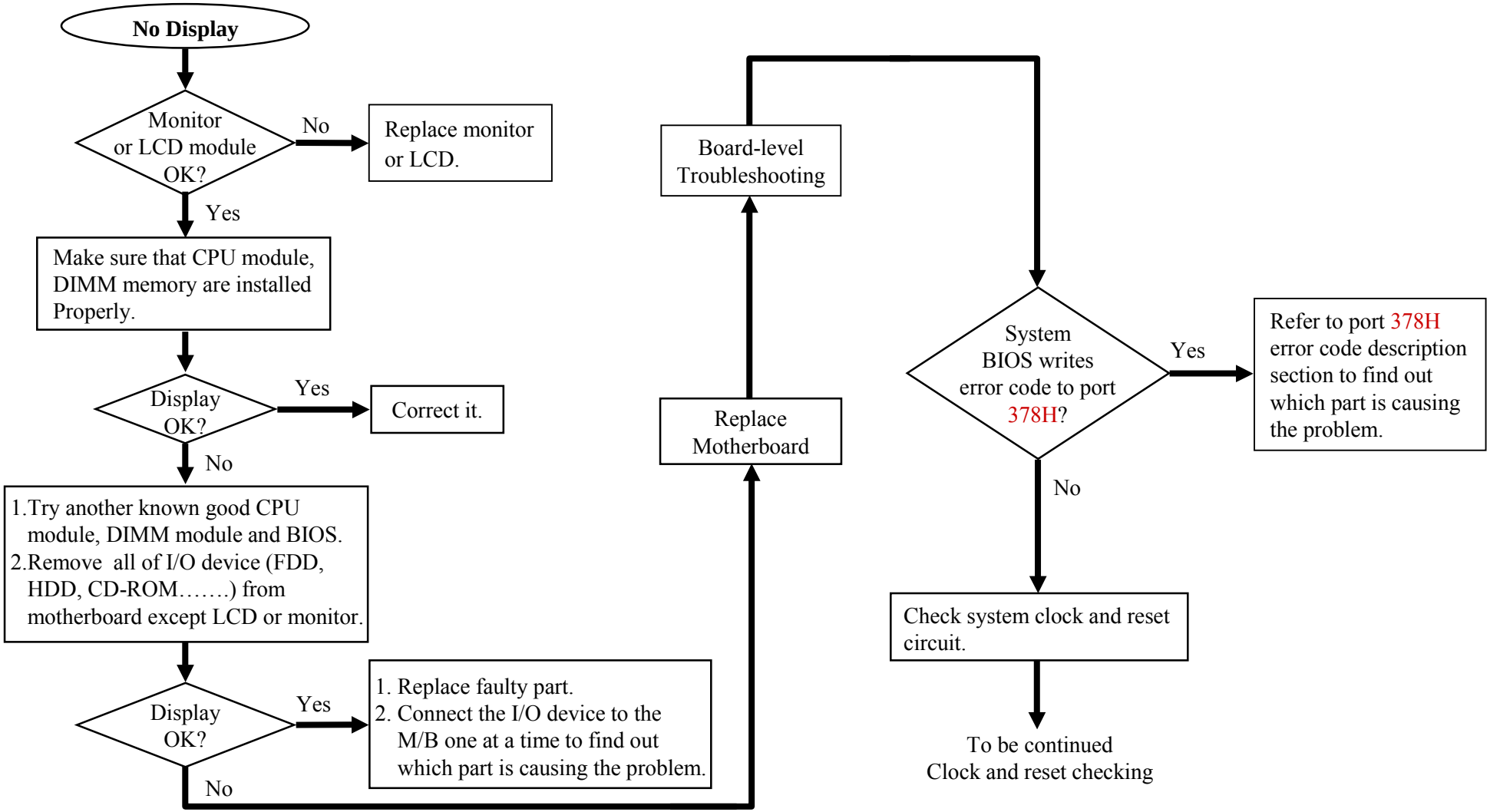
8.1 No Power – Battery Discharge

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.2 No Display

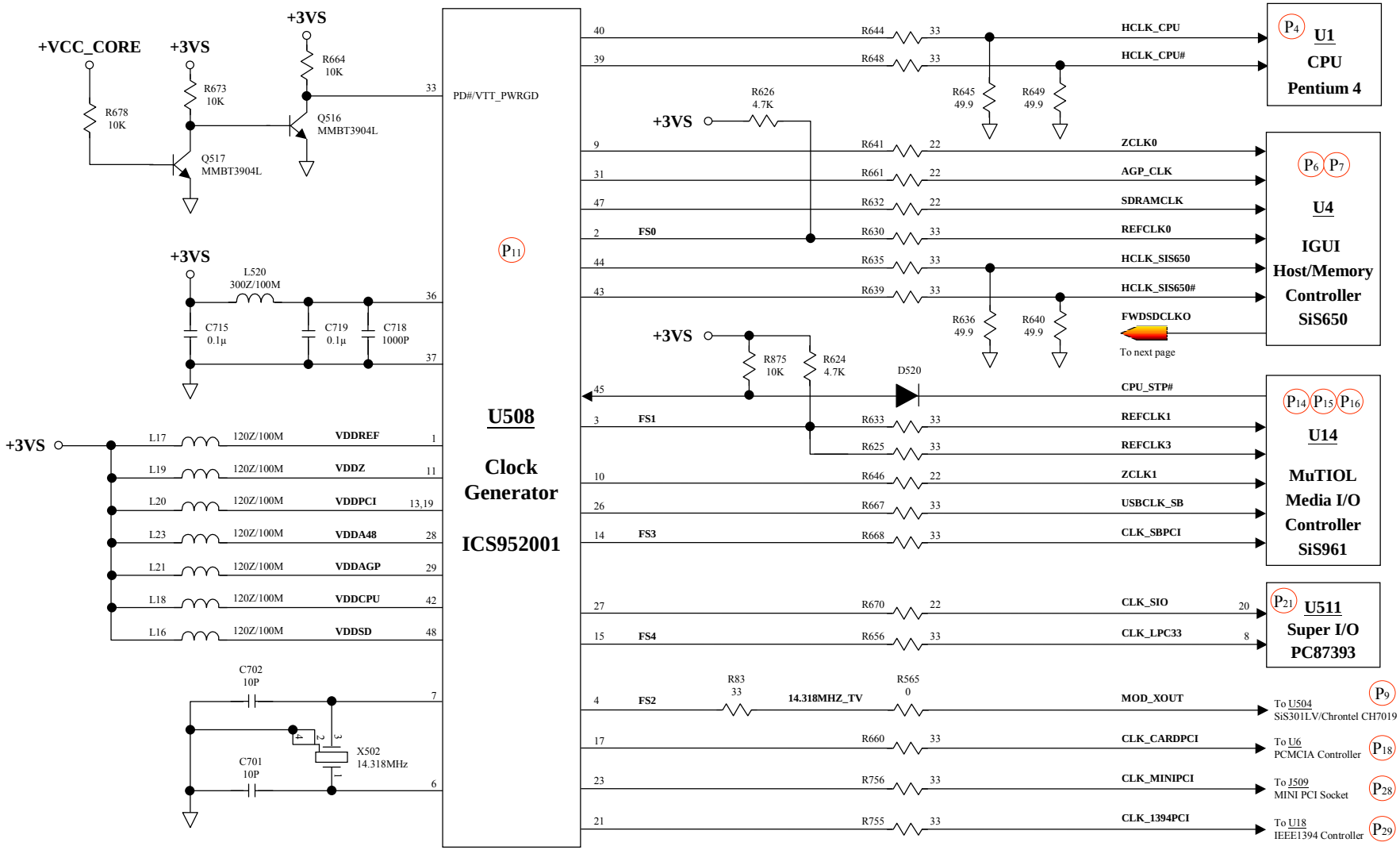
There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.


No Display
Monitor or LCD module OK?
No
Replace monitor or LCD.
Yes
Make sure that CPU module, DIMM memory are installed Properly.
Display OK?
Yes
Correct it.
No
1.Try another known good CPU module, DIMM module and BIOS.
2.Remove all of I/O device (FDD, HDD, CD-ROM…….) from motherboard except LCD or monitor.
Display OK?
Yes
1. Replace faulty part.
2. Connect the I/O device to the M/B one at a time to find out which part is causing the problem.
No
Replace Motherboard
Board-level Troubleshooting
System BIOS writes error code to port 378H?
Yes
Refer to port 378H error code description section to find out which part is causing the problem.
No
Check system clock and reset circuit.
To be continued
Clock and reset checking

8575 N/B Maintenance

8.2 No Display

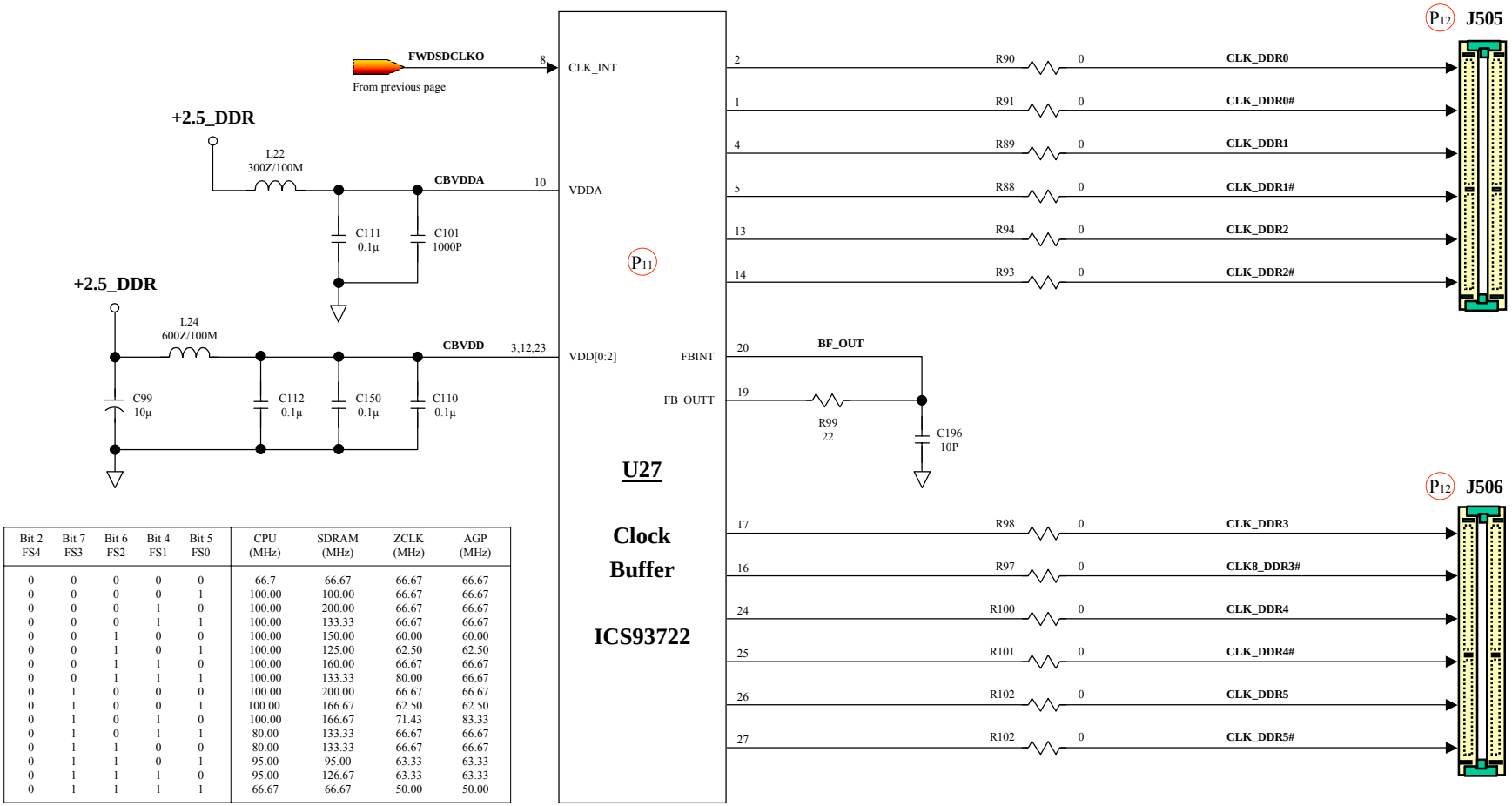
****** System Clock Check ******



8575 N/B Maintenance

8.2 No Display

****** System Clock Check ******

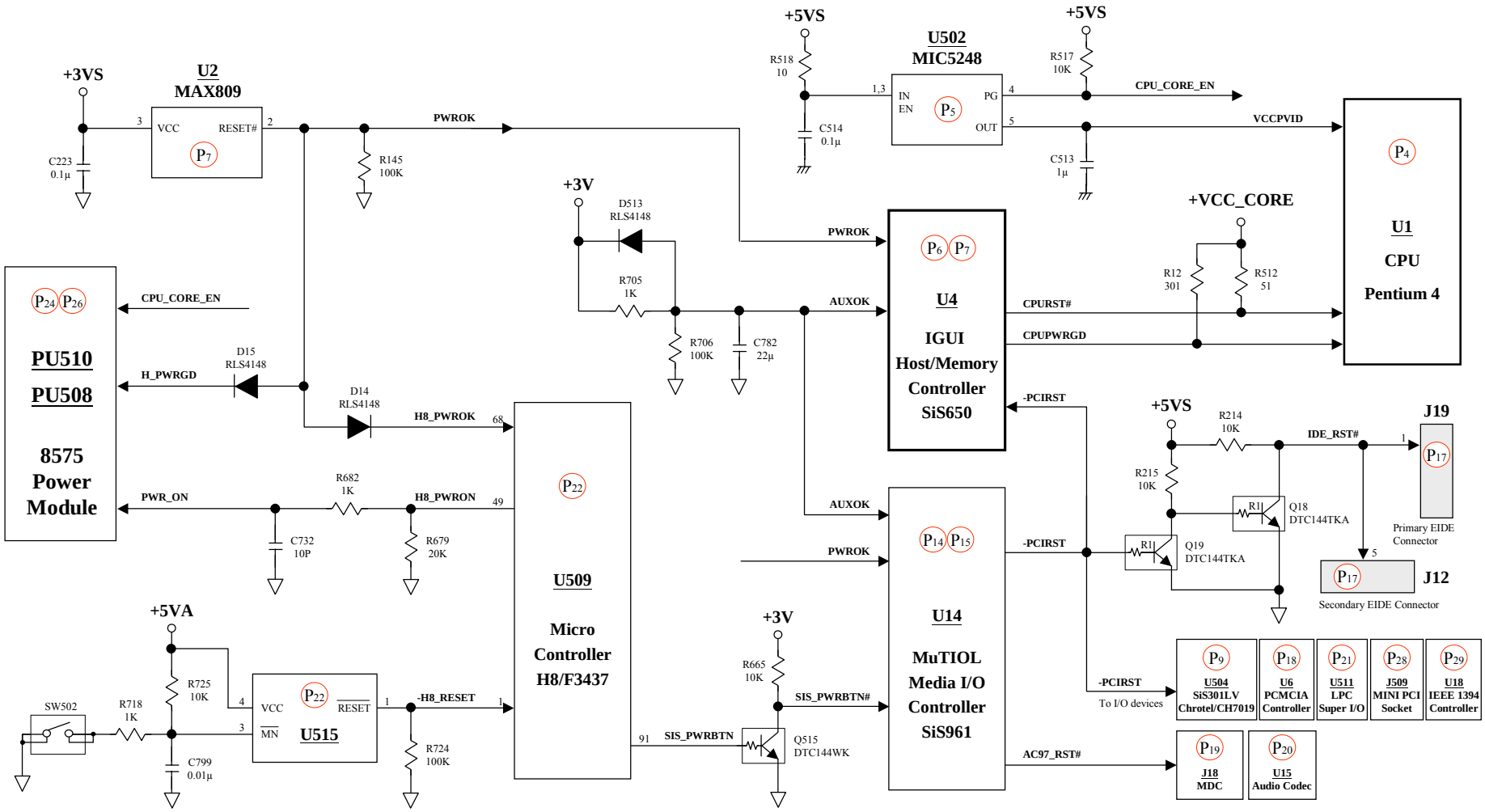


Bit 2 FS4	Bit 7 FS3	Bit 6 FS2	Bit 4 FS1	Bit 5 FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGP (MHz)
0	0	0	0	0	66.7	66.67	66.67	66.67
0	0	0	0	1	100.00	100.00	66.67	66.67
0	0	0	1	0	100.00	200.00	66.67	66.67
0	0	0	1	1	100.00	133.33	66.67	66.67
0	0	1	0	0	100.00	150.00	60.00	60.00
0	0	1	0	1	100.00	125.00	62.50	62.50
0	0	1	1	0	100.00	160.00	66.67	66.67
0	0	1	1	1	100.00	133.33	80.00	66.67
0	1	0	0	0	100.00	200.00	66.67	66.67
0	1	0	0	1	100.00	166.67	62.50	62.50
0	1	0	1	0	100.00	166.67	71.43	83.33
0	1	0	1	1	80.00	133.33	66.67	66.67
0	1	1	0	0	80.00	133.33	66.67	66.67
0	1	1	0	1	95.00	95.00	63.33	63.33
0	1	1	1	0	95.00	126.67	63.33	63.33
0	1	1	1	1	66.67	66.67	50.00	50.00

8575 N/B Maintenance

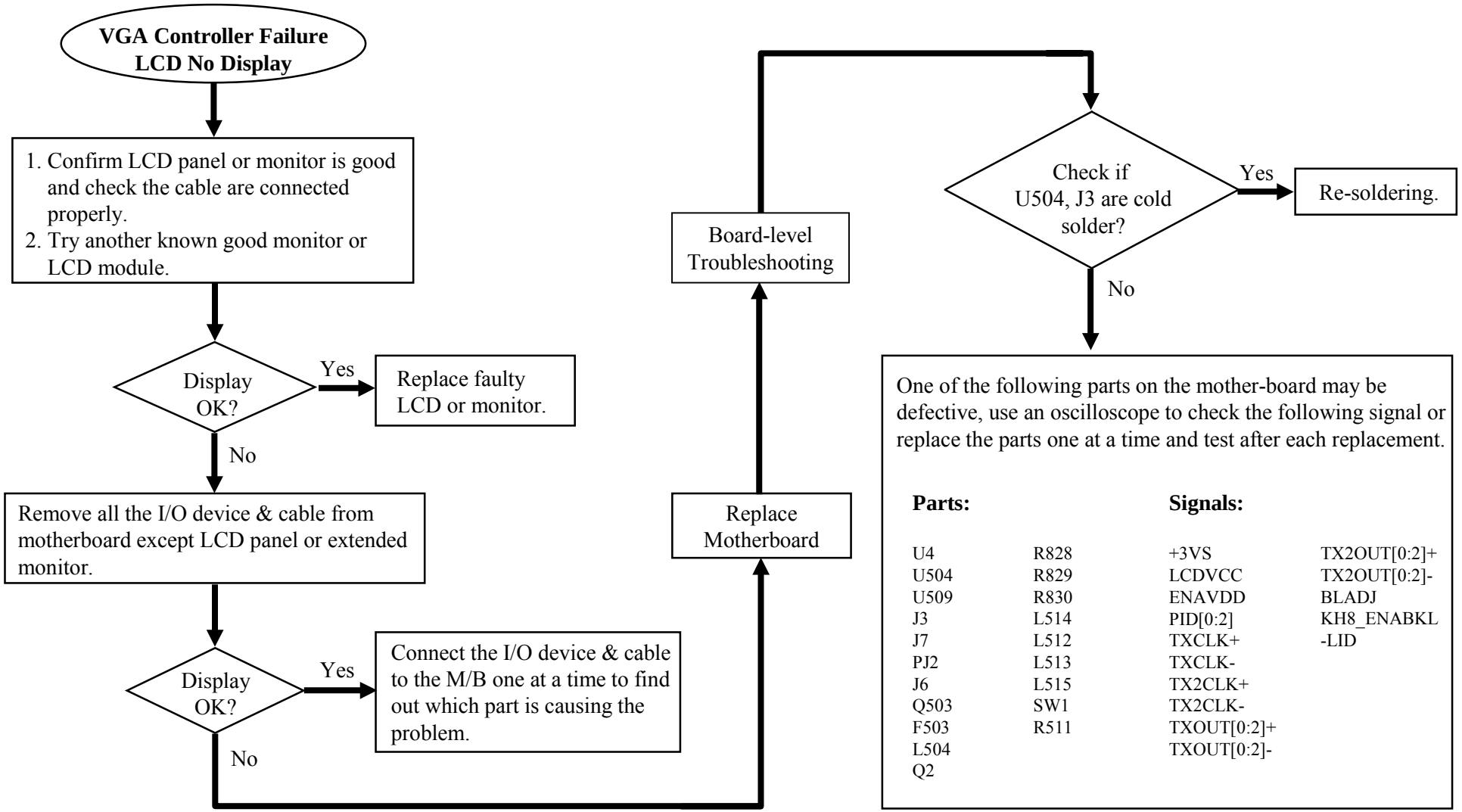
8.2 No Display

****** Power Good & Reset Circuit Check ******



8.3 VGA Controller Failure LCD No Display

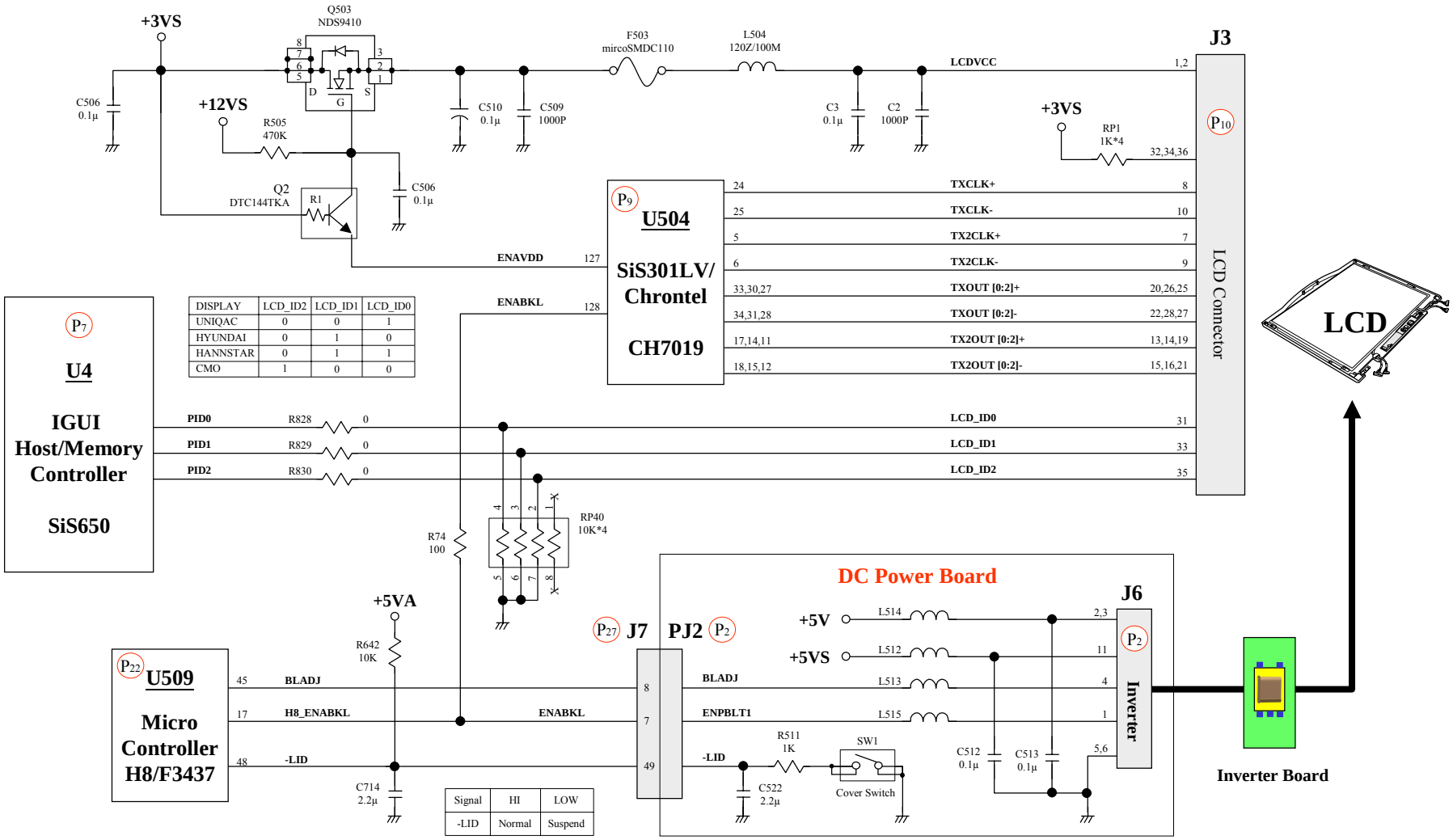
There is no display or picture abnormal on LCD although power-on-self-test is passed.



8575 N/B Maintenance

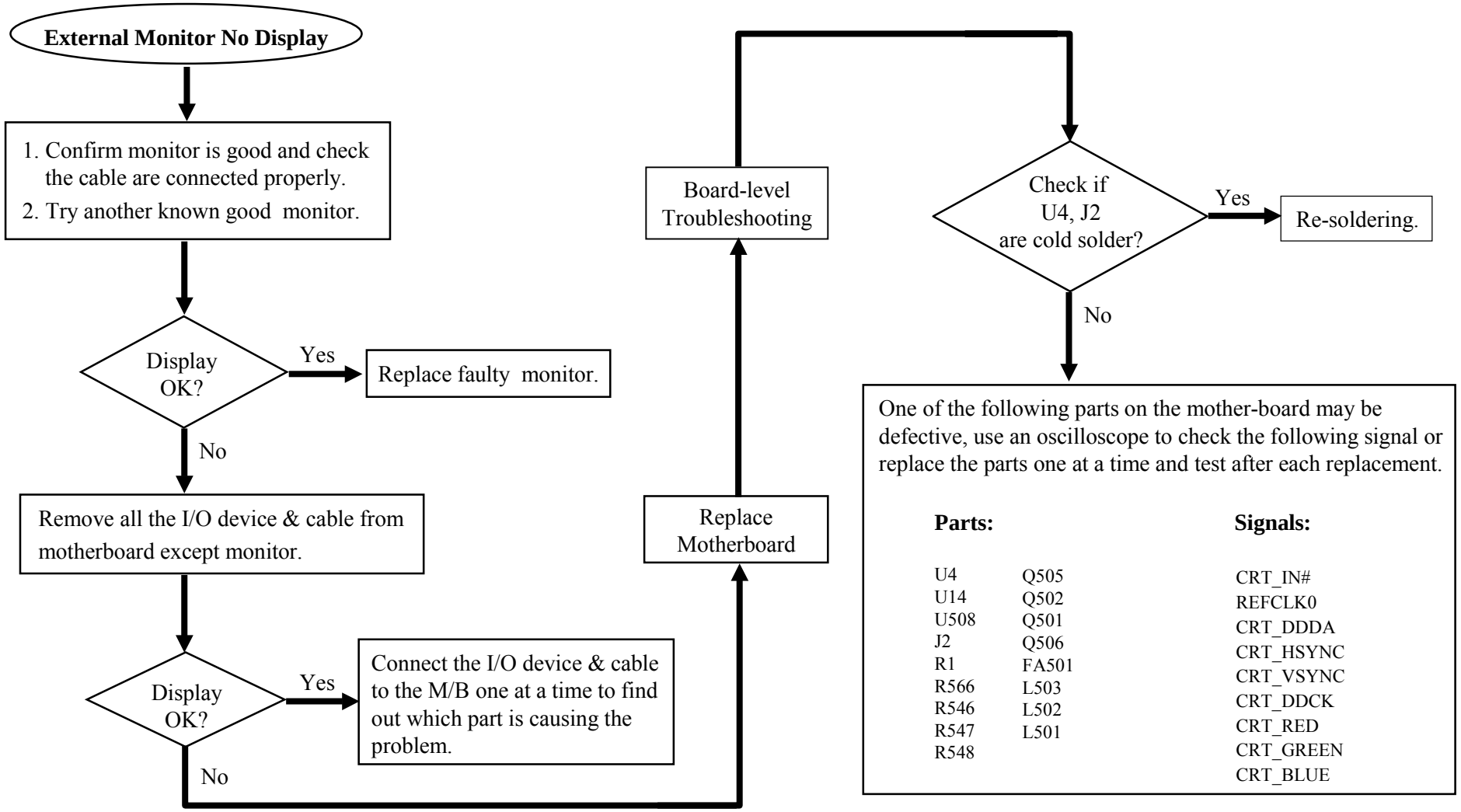
8.3 VGA Controller Failure LCD No Display

There is no display or picture abnormal on LCD although power-on-self-test is passed.



8.4 External Monitor No Display

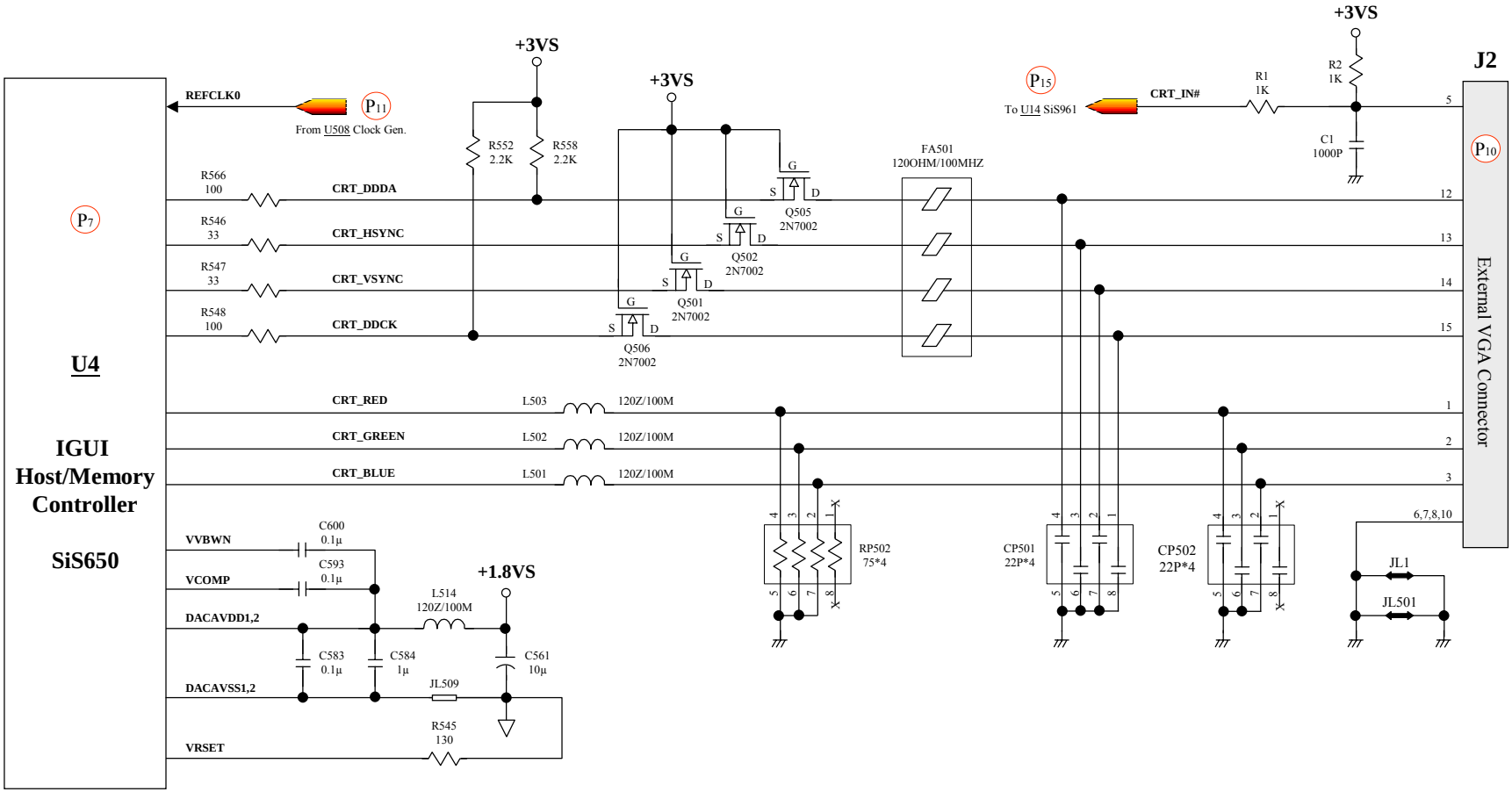
There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8575 N/B Maintenance

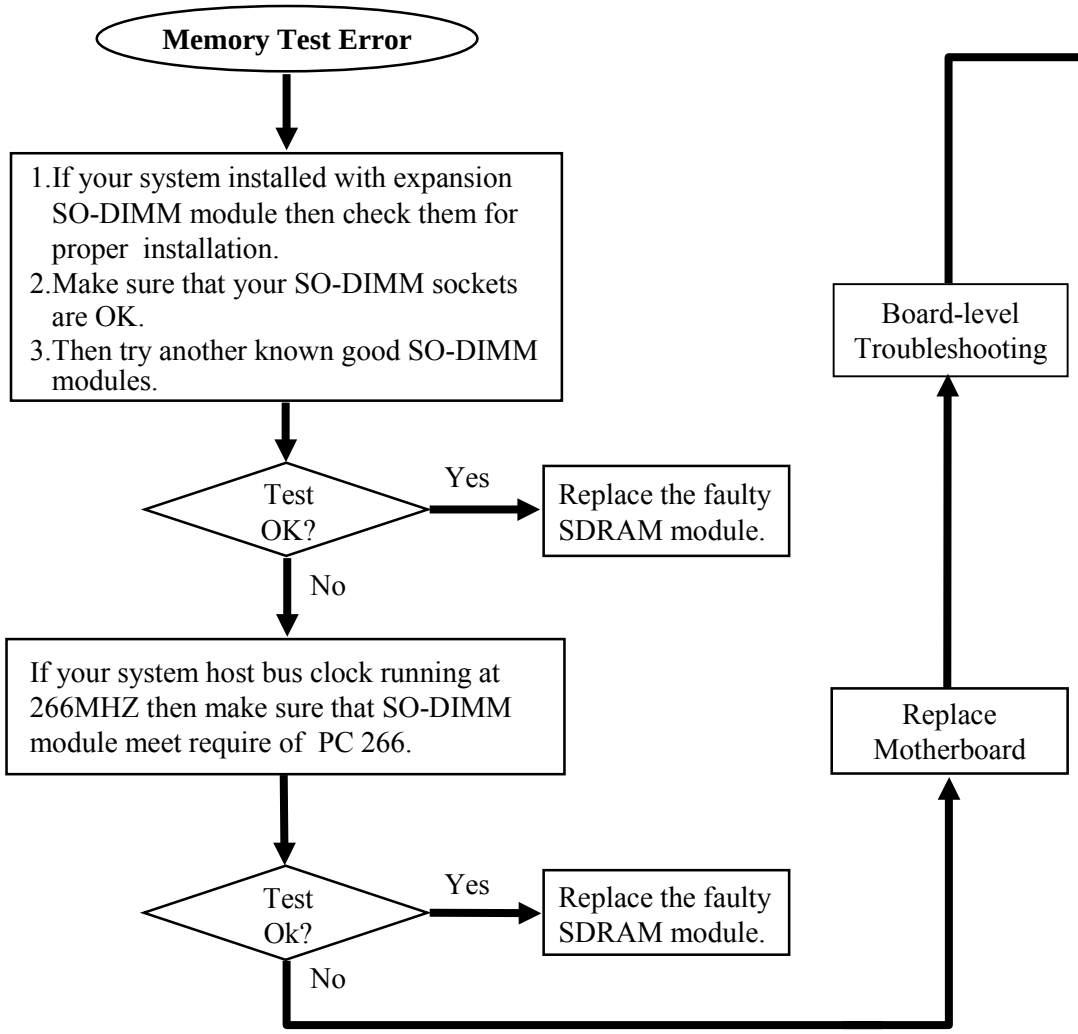
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8.5 Memory Test Error

Extend SDRAM is failure or system hangs up.


Memory Test Error
1.If your system installed with expansion SO-DIMM module then check them for proper installation.
2.Make sure that your SO-DIMM sockets are OK.
3.Then try another known good SO-DIMM modules.
Test OK?
Yes
Replace the faulty SDRAM module.
No
If your system host bus clock running at 266MHZ then make sure that SO-DIMM module meet require of PC 266.
Test Ok?
Yes
Replace the faulty SDRAM module.
No
Replace Motherboard
Board-level Troubleshooting

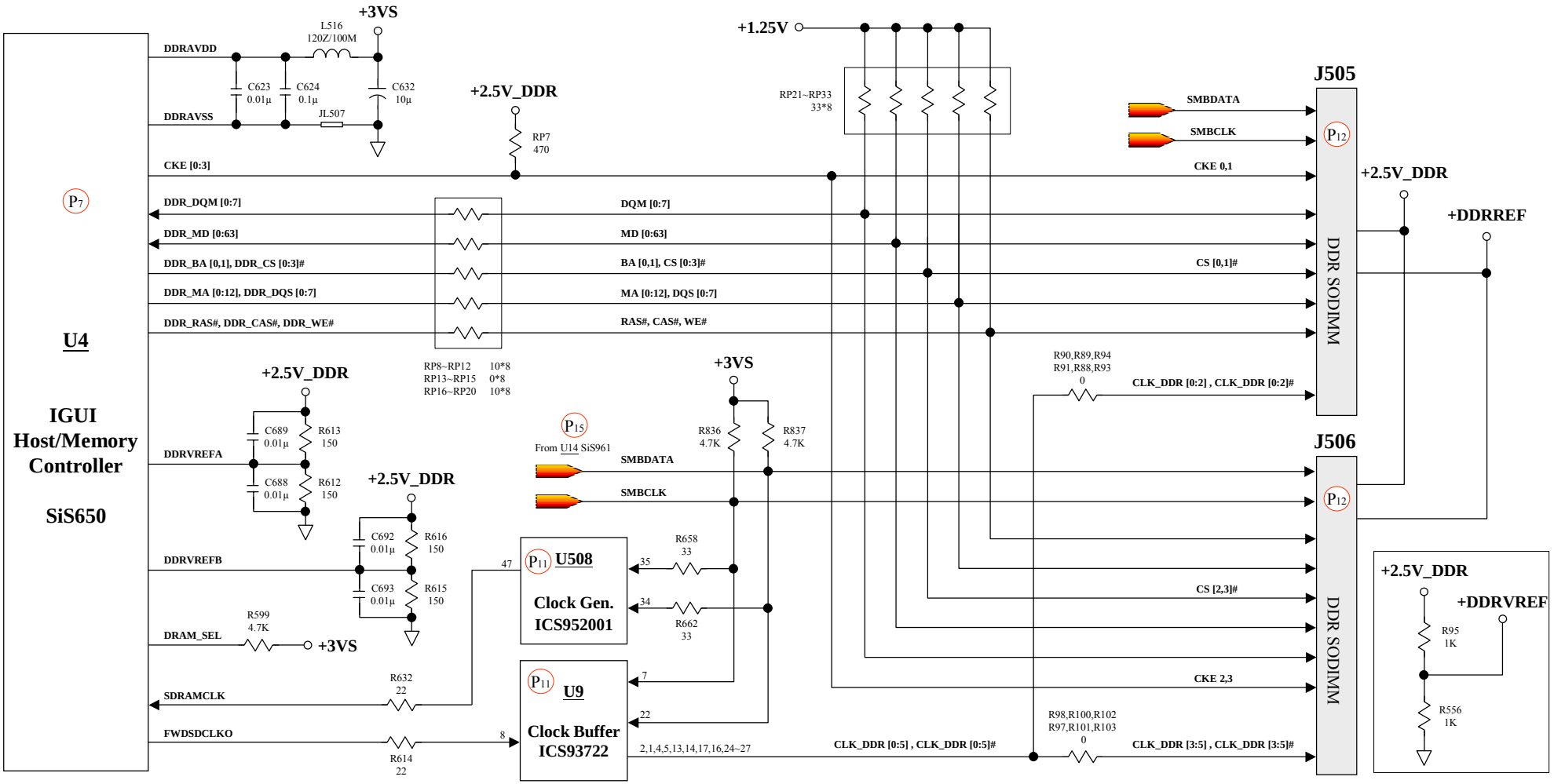
One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.

Parts:		**Signals:**
U4	R90	+2.5V_DDR
U508	R91	+DDRVREF
U9	R98	CKE[0:3]
J505	R88	DDR_DQM[0:7]
J506	R94	DDR_MD[0:63]
RP8~RP12	R93	DDR_BA [0,1]
RP13~RP15		DDR_CS[0:3]#
RP16~RP20		DDR_MA[0:12]
R632		DDR_DQS[0:7]
R614		DDR_RAS#
R658		DDR_CAS#
R662		DDR_WE#
R98		SDRAMCLK
R100		FWDSDCLK
R102		SMBDATA
R97		SMBCLK
R101		CLK_DDR[0:5]
R103		CLK_DDR[0:5]#

8575 N/B Maintenance

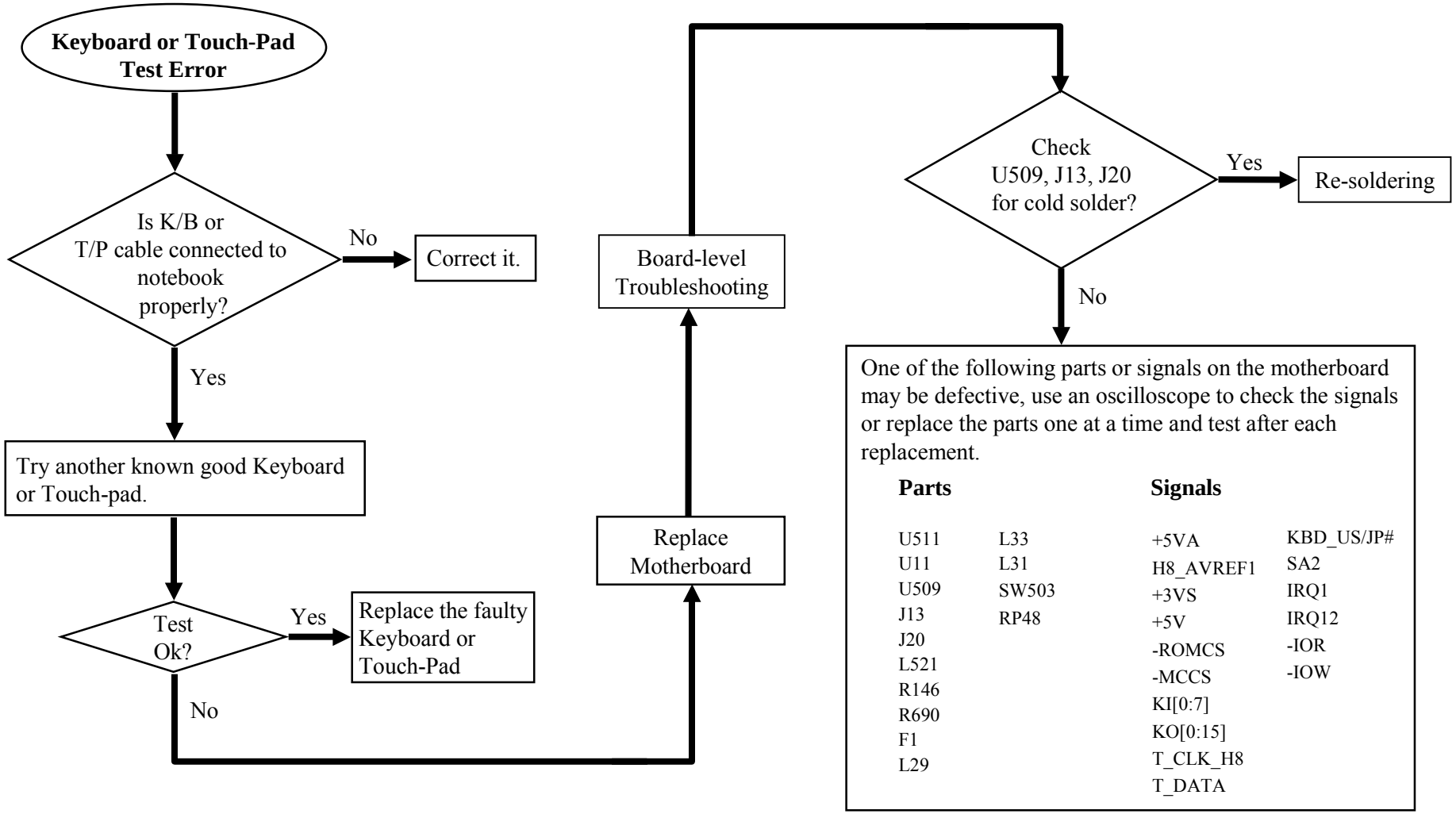
8.5 Memory Test Error

Extend SDRAM is failure or system hangs up.



8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

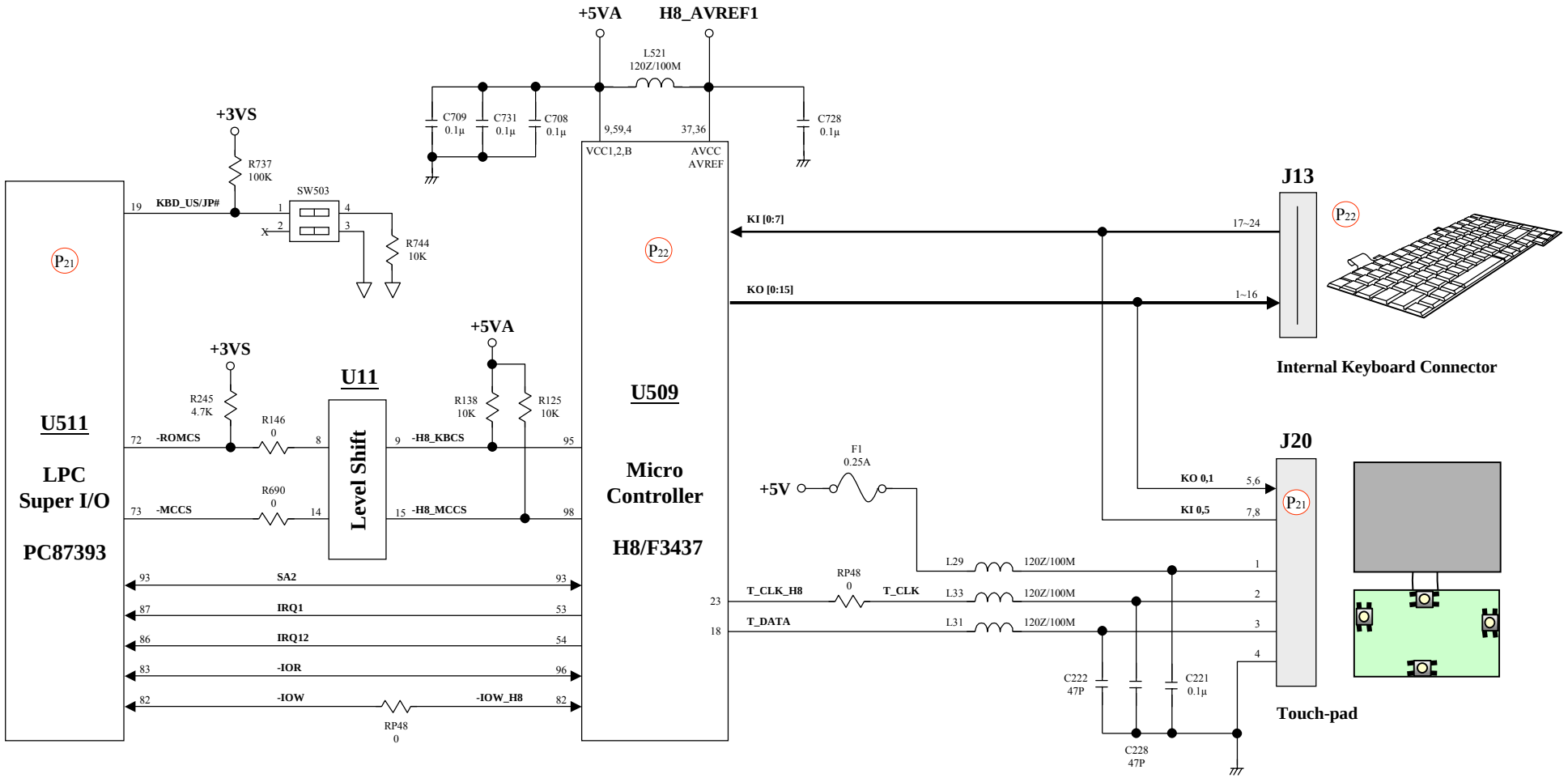
Error message of keyboard or touch-pad failure is shown or any key does not work.



8575 N/B Maintenance

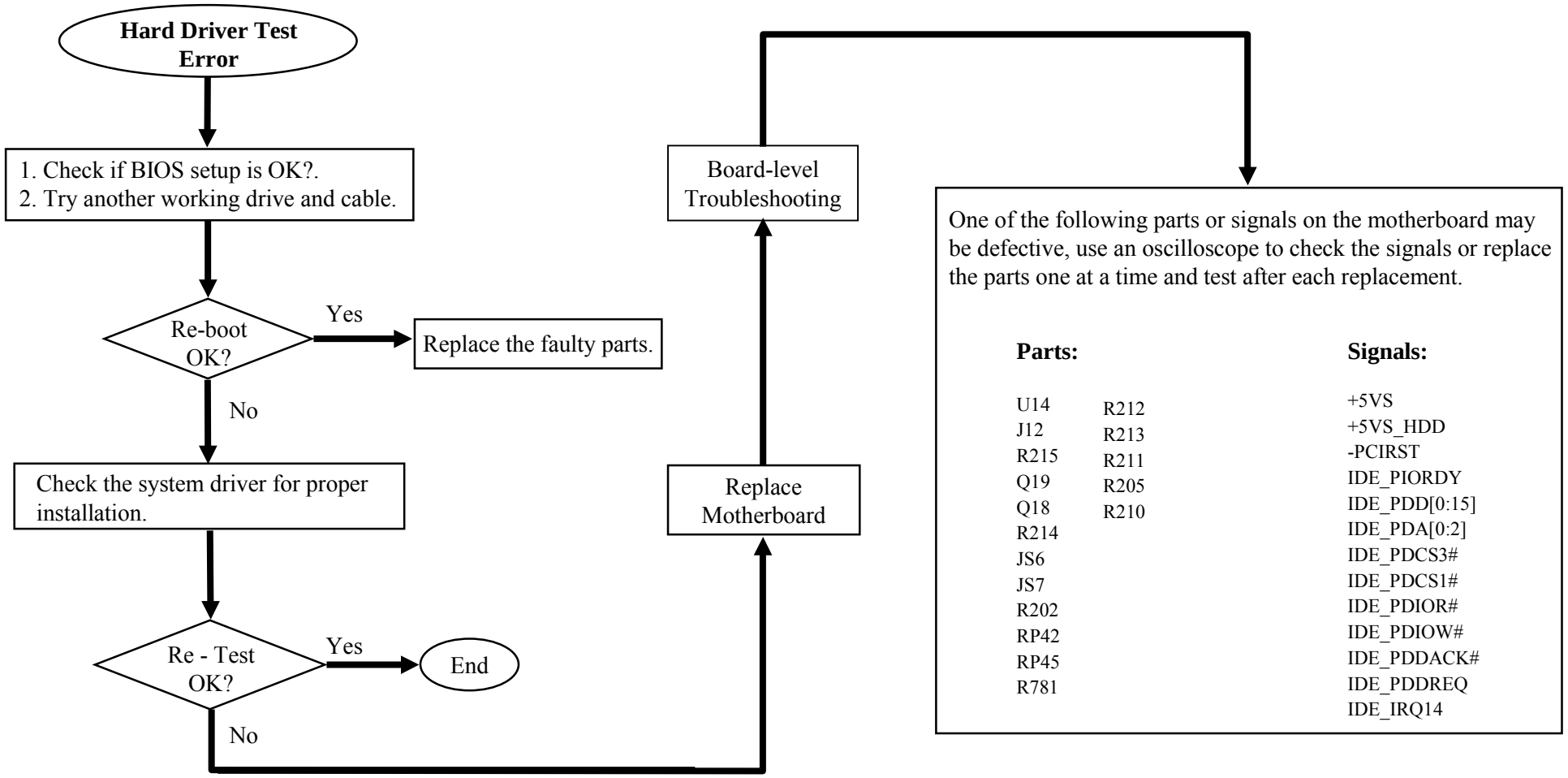
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



8.7 Hard Drive Test Error

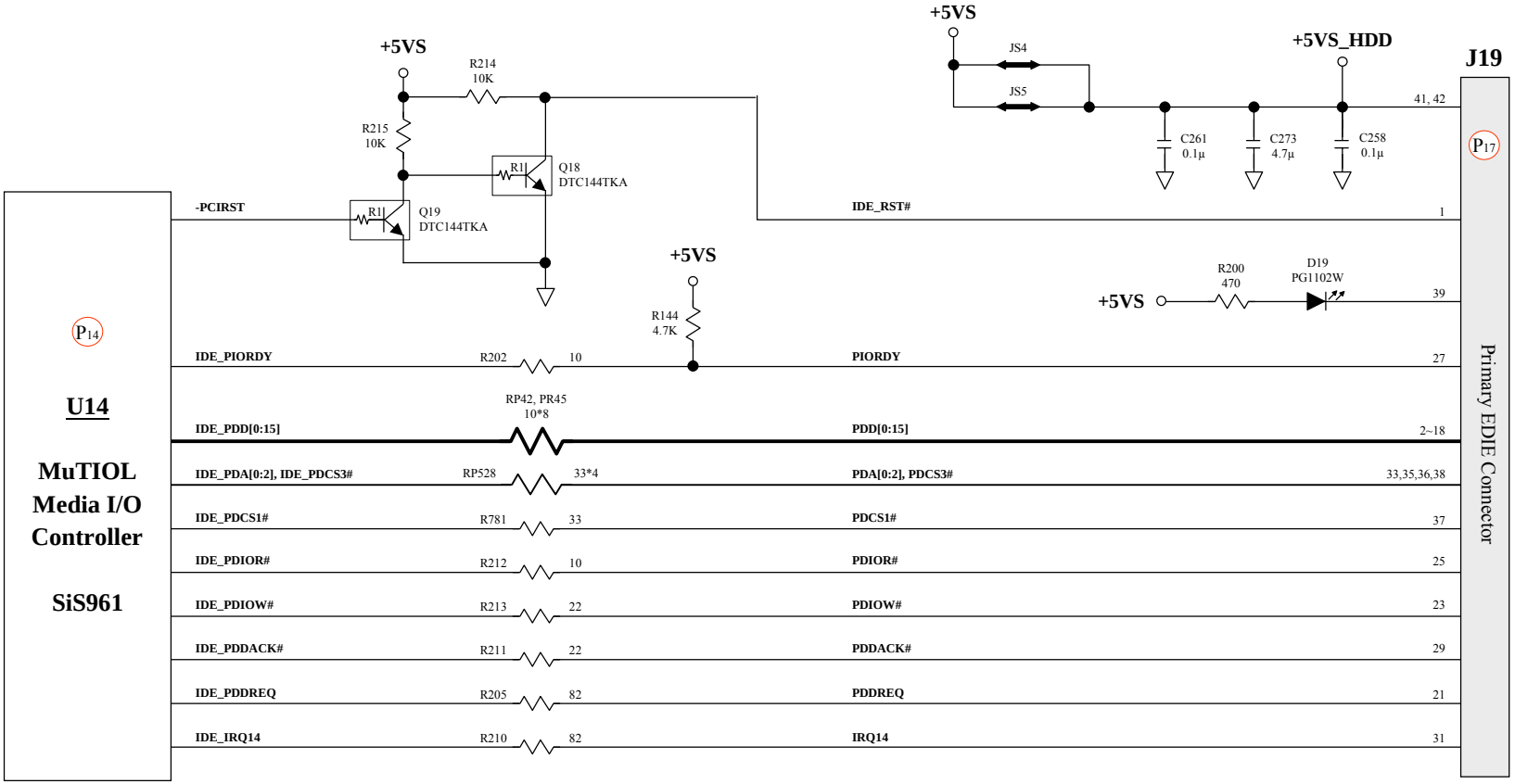
Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8575 N/B Maintenance

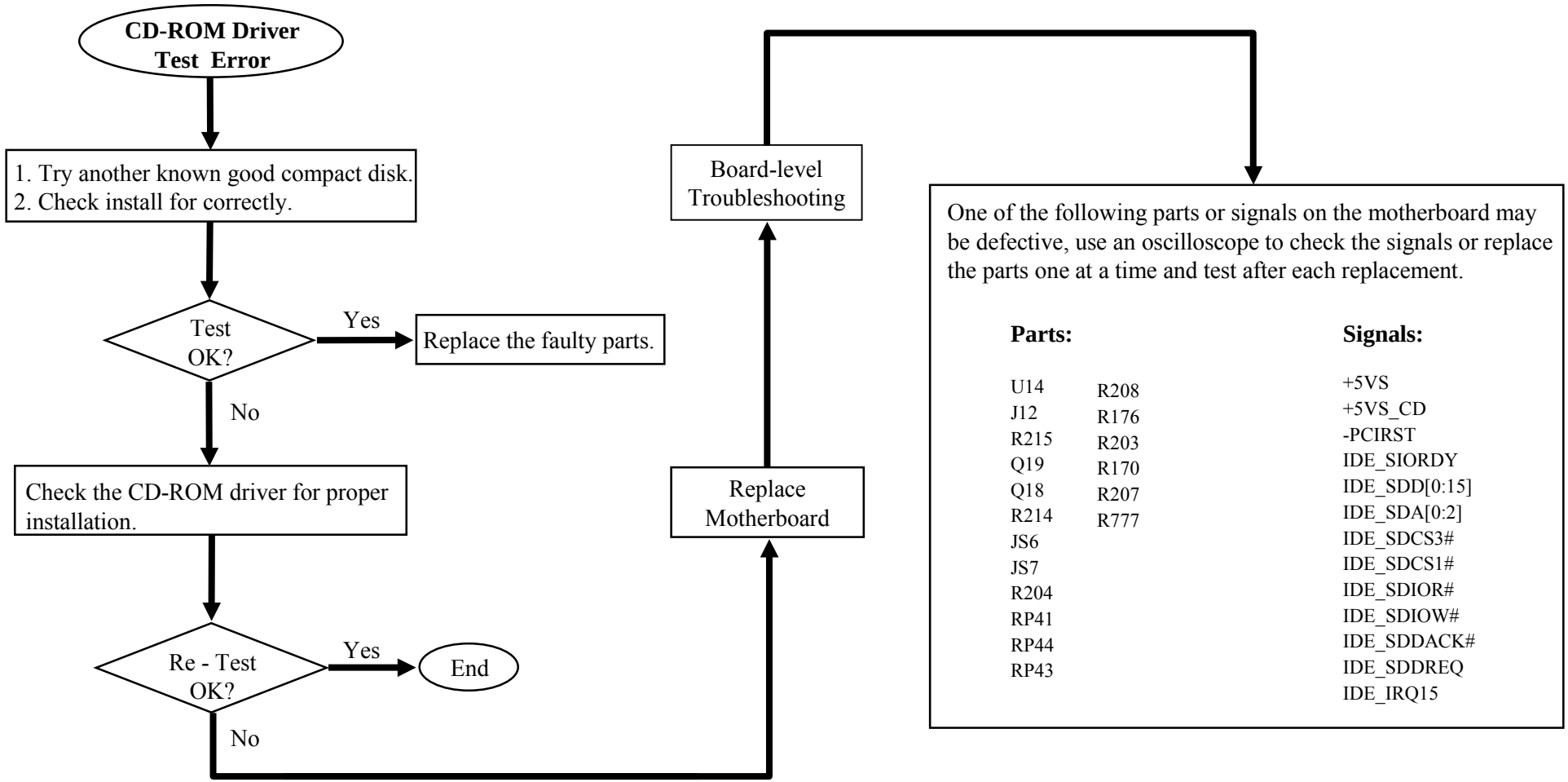
8.7 Hard Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8.8 CD-ROM Drive Test Error

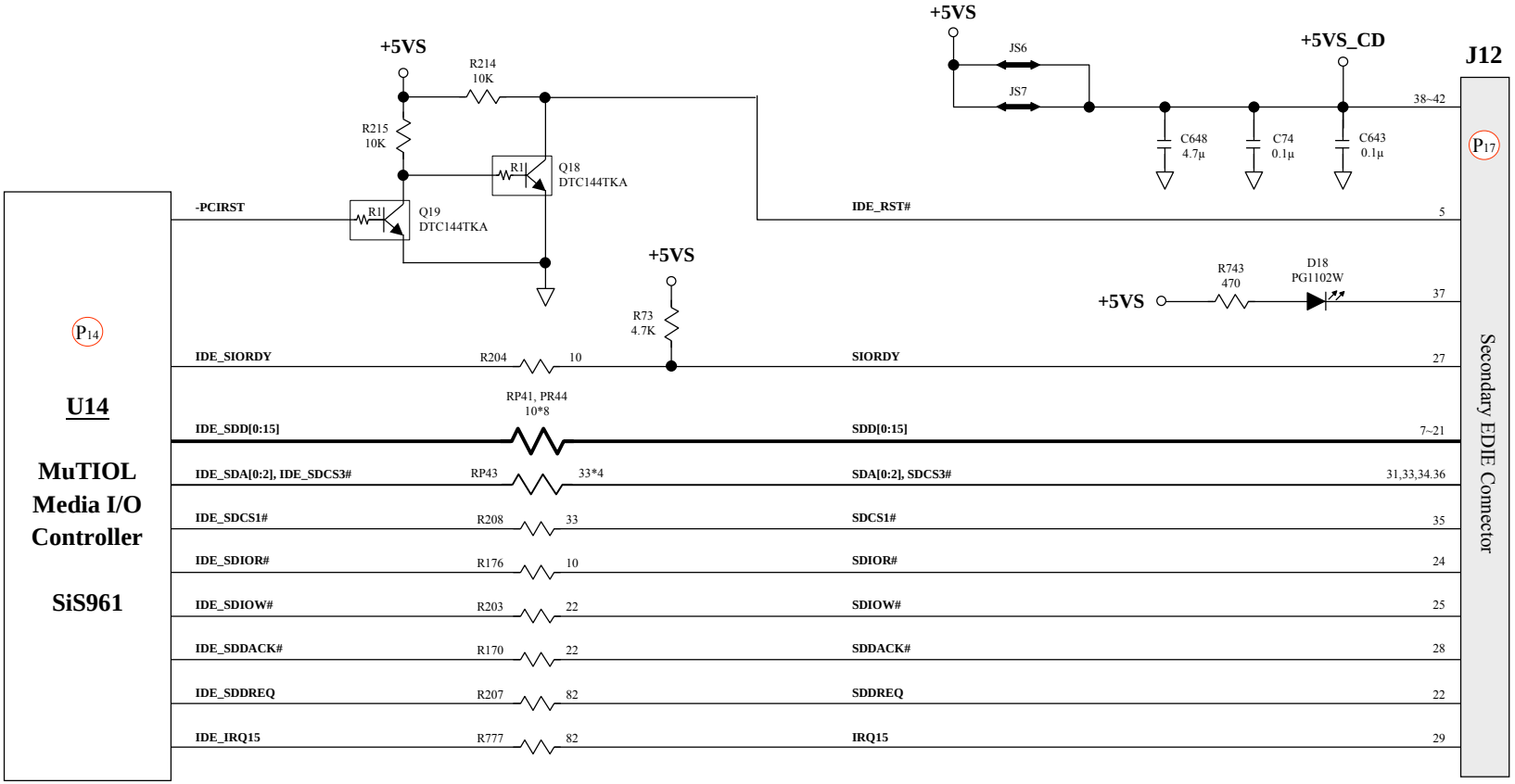
An error message is shown when reading data from CD-ROM drive.



8575 N/B Maintenance

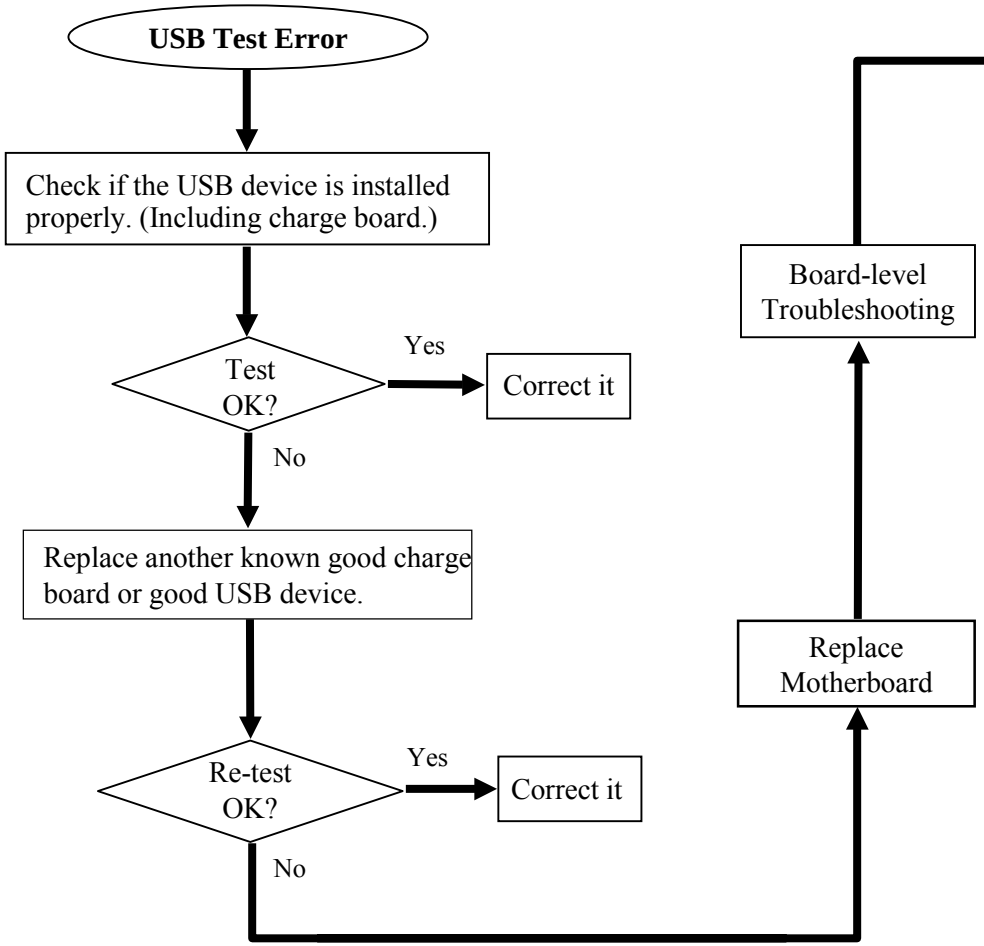
8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



8.9 USB Test Error

An error occurs when a USB I/O device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

M/B	D/D	
U14	PJ2	U1
J7	JU3	J8
R147	J5	J4
R148	J7	D3
R75	D504	L520
R518	L524	L522
R142	L509	L504
R143	L516	L508
R161	L518	
R163		

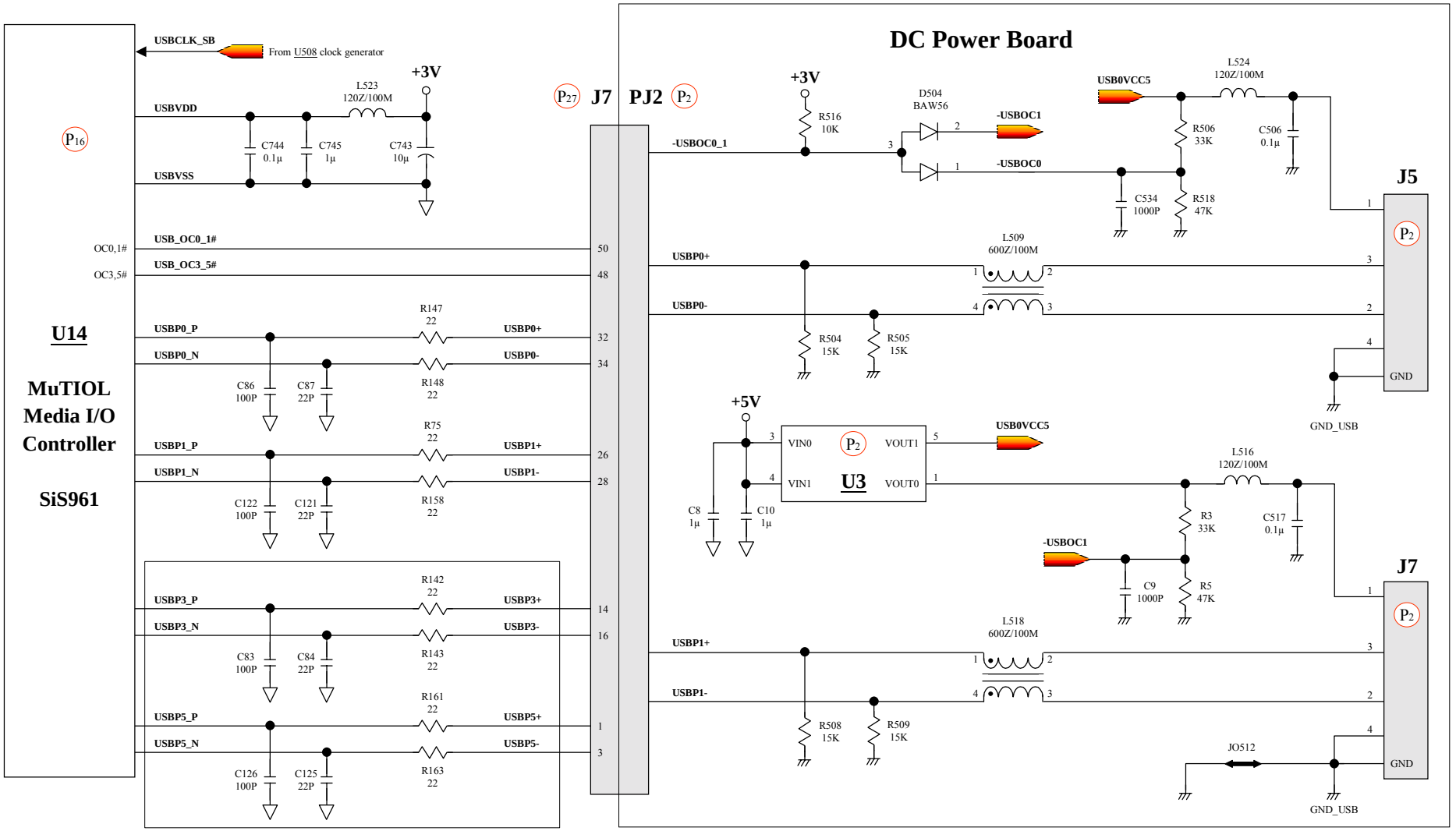
Signals:

+3V	-USBOC3_5
USBCLK_SB	USBP5+
-USBOC0_1	USBP5-
USBP0+	USB5VCC5
USBP0-	USBP3+
USB0VCC5	USBP3-
USBP1+	
USBP1-	

8575 N/B Maintenance

8.9 USB Test Error - 1

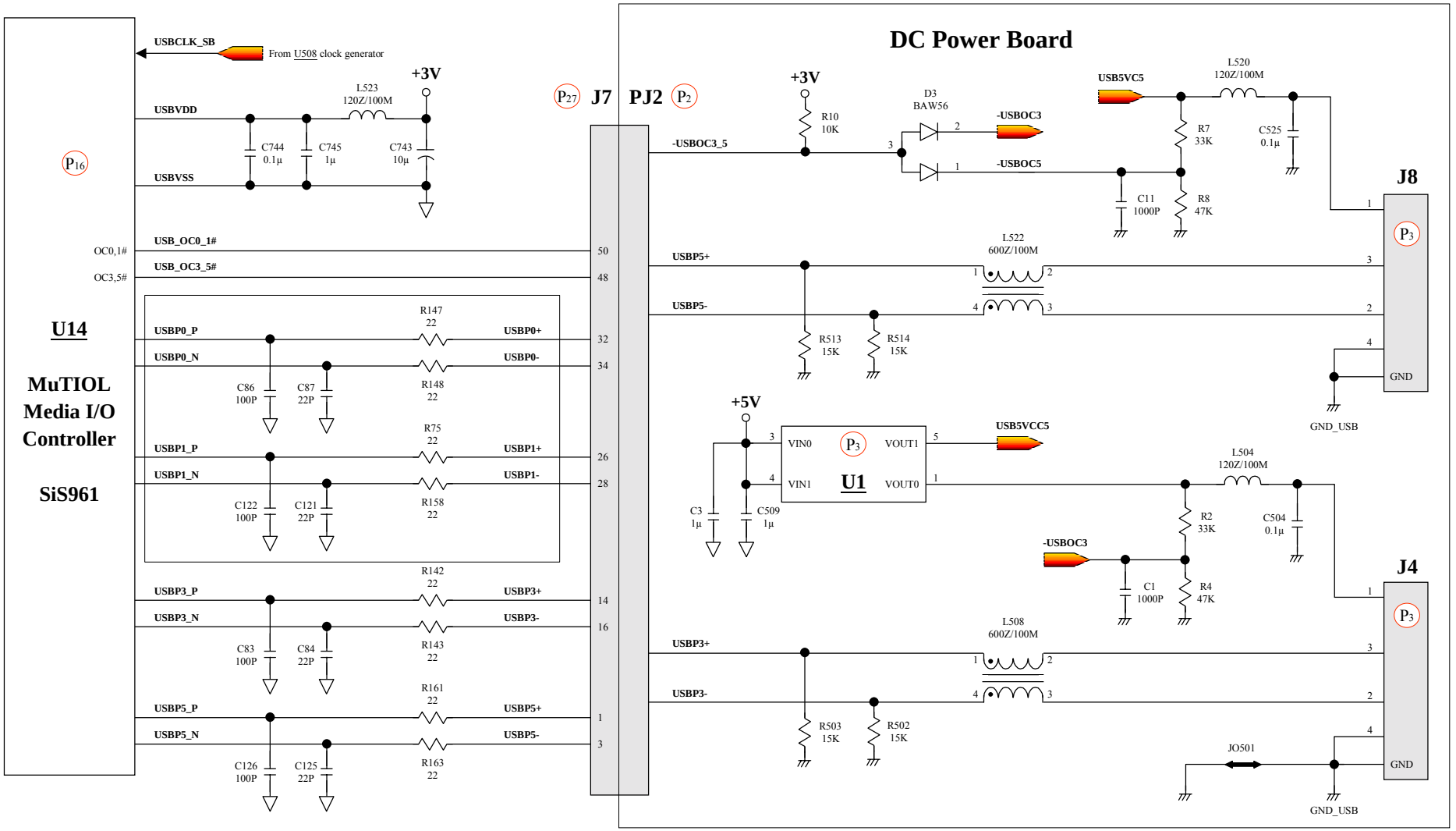
An error occurs when a USB I/O device is installed.



8575 N/B Maintenance

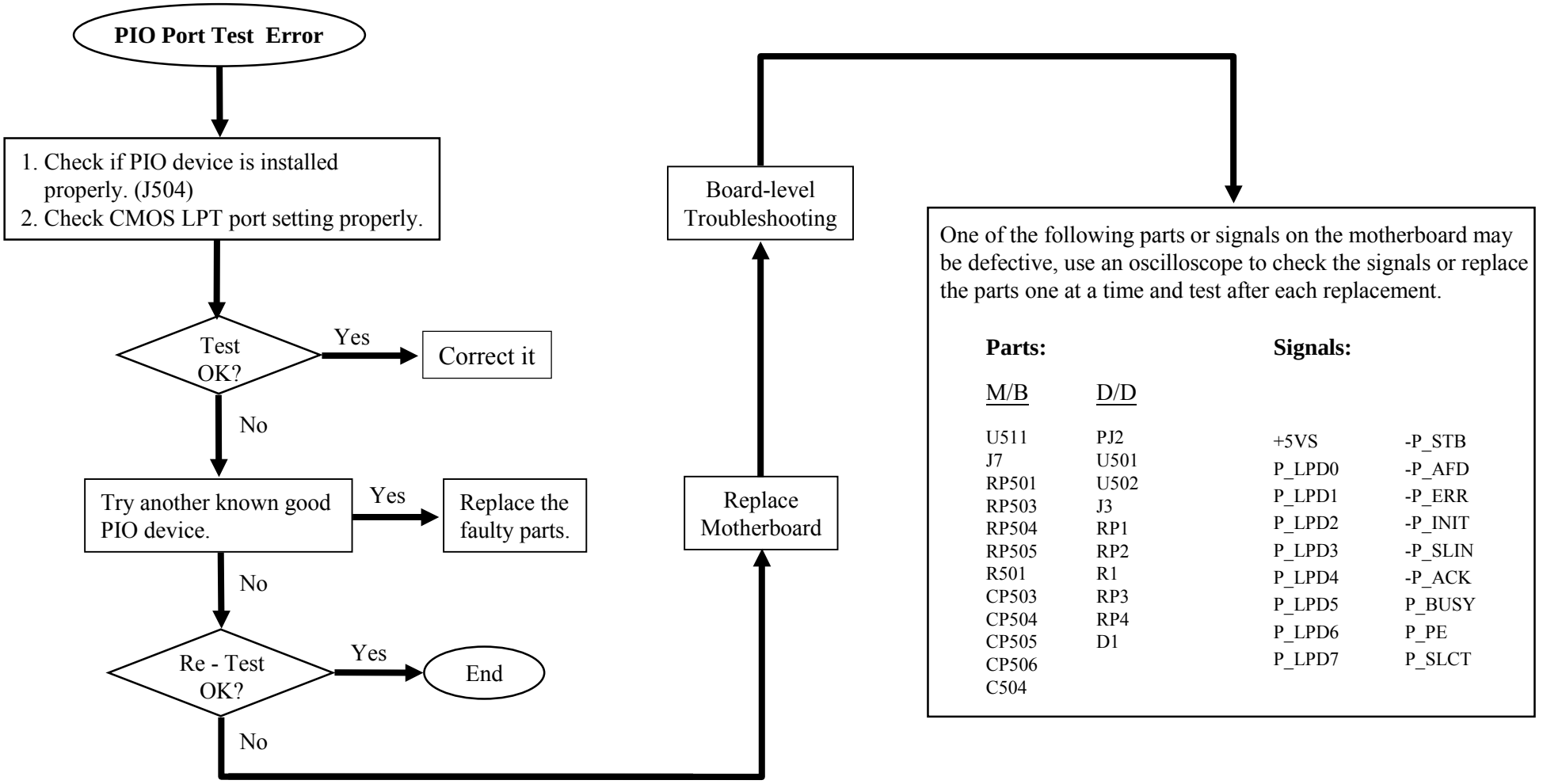
8.9 USB Test Error - 2

An error occurs when a USB I/O device is installed.



8.10 PIO Port Test Error

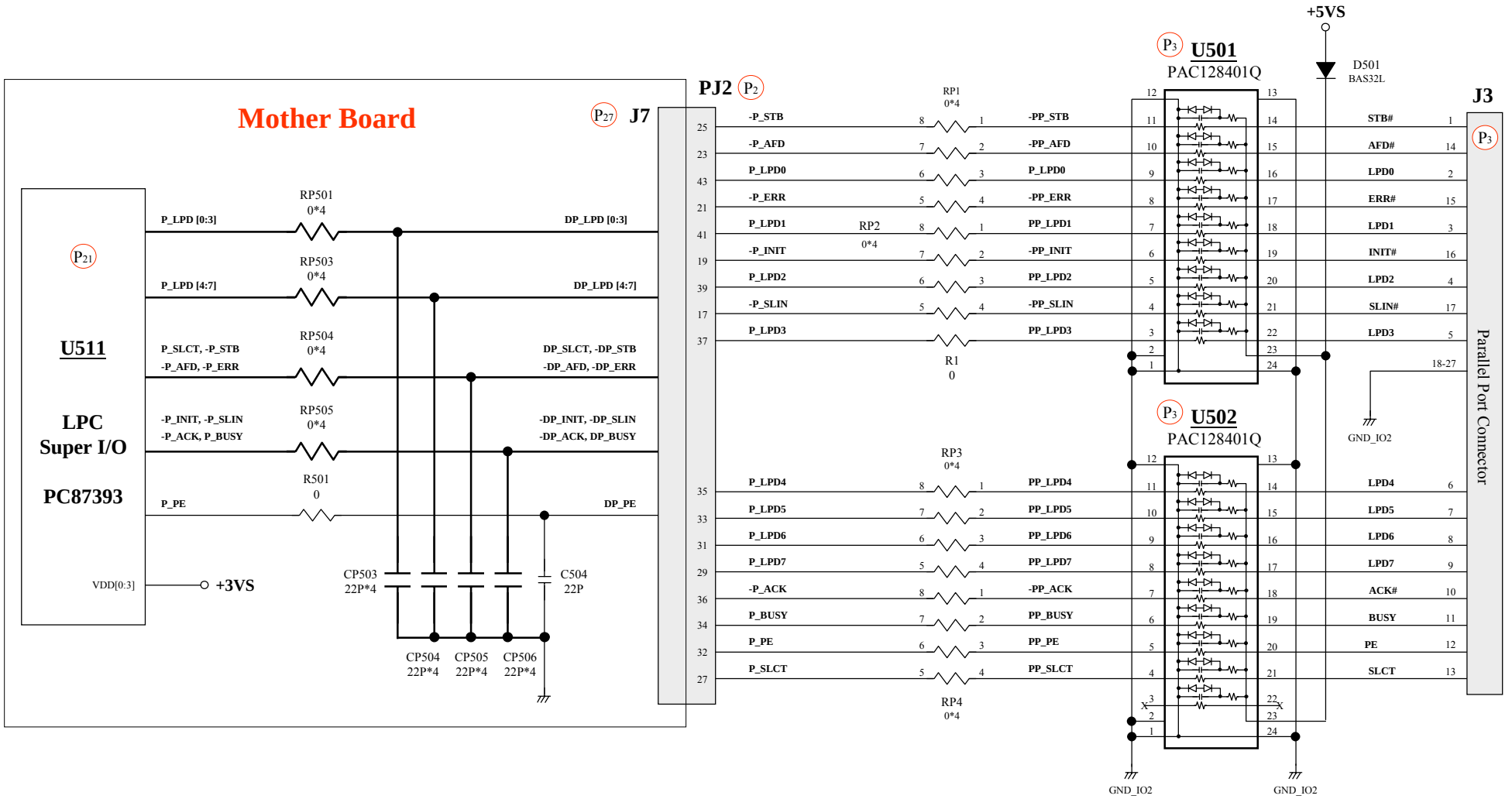
When a print command is issued, printer prints nothing or garbage.



8575 N/B Maintenance

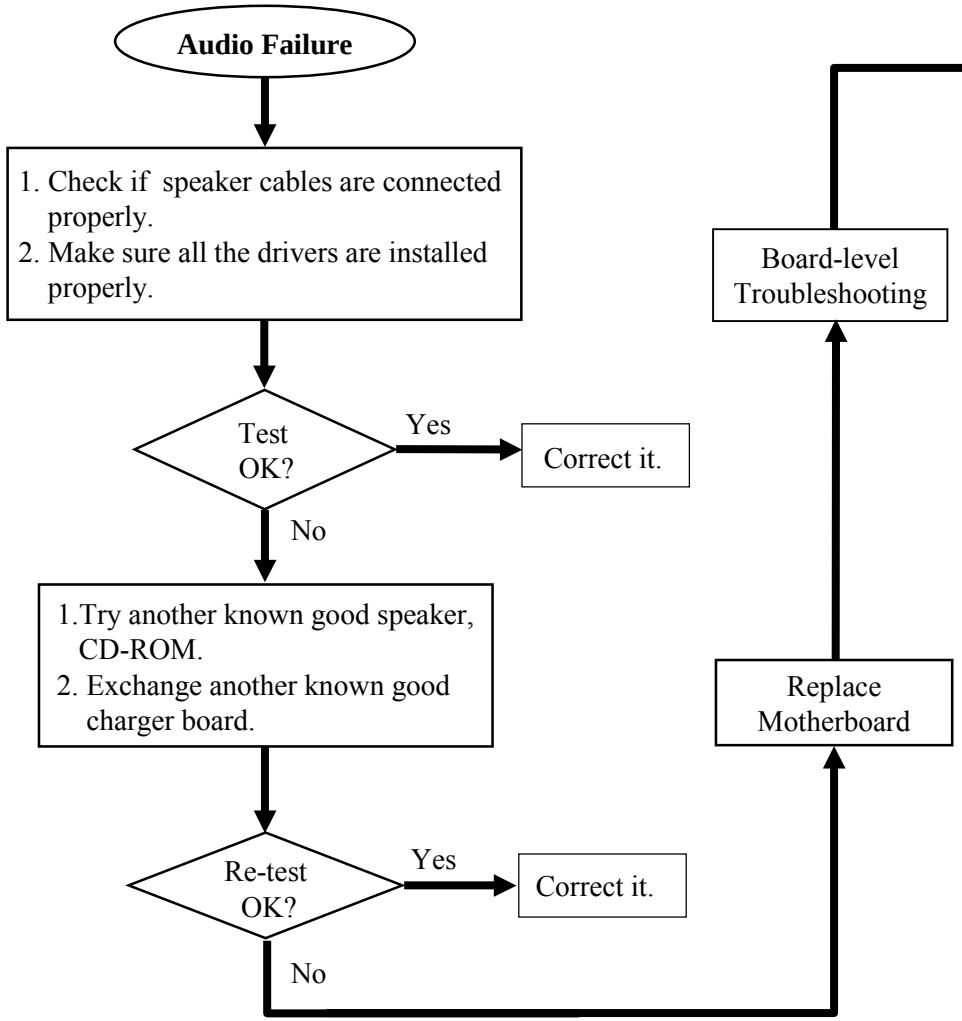
8.10 PIO Port Test Error

When a print command is issued, printer prints nothing or garbage.



8.11 Audio Failure

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U14	AOUT_R
U15	AOUT_L
U16	+3VS
VR1	5V_AMP
L529	+3VS_SPD
L28	SPK_OFF
L530	SPDIFOUT
Q528	
Q529	
J24	

2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U14	+5VS
U15	AVDDAD
J21	MIC1
J28	
C272	
L531	
L532	

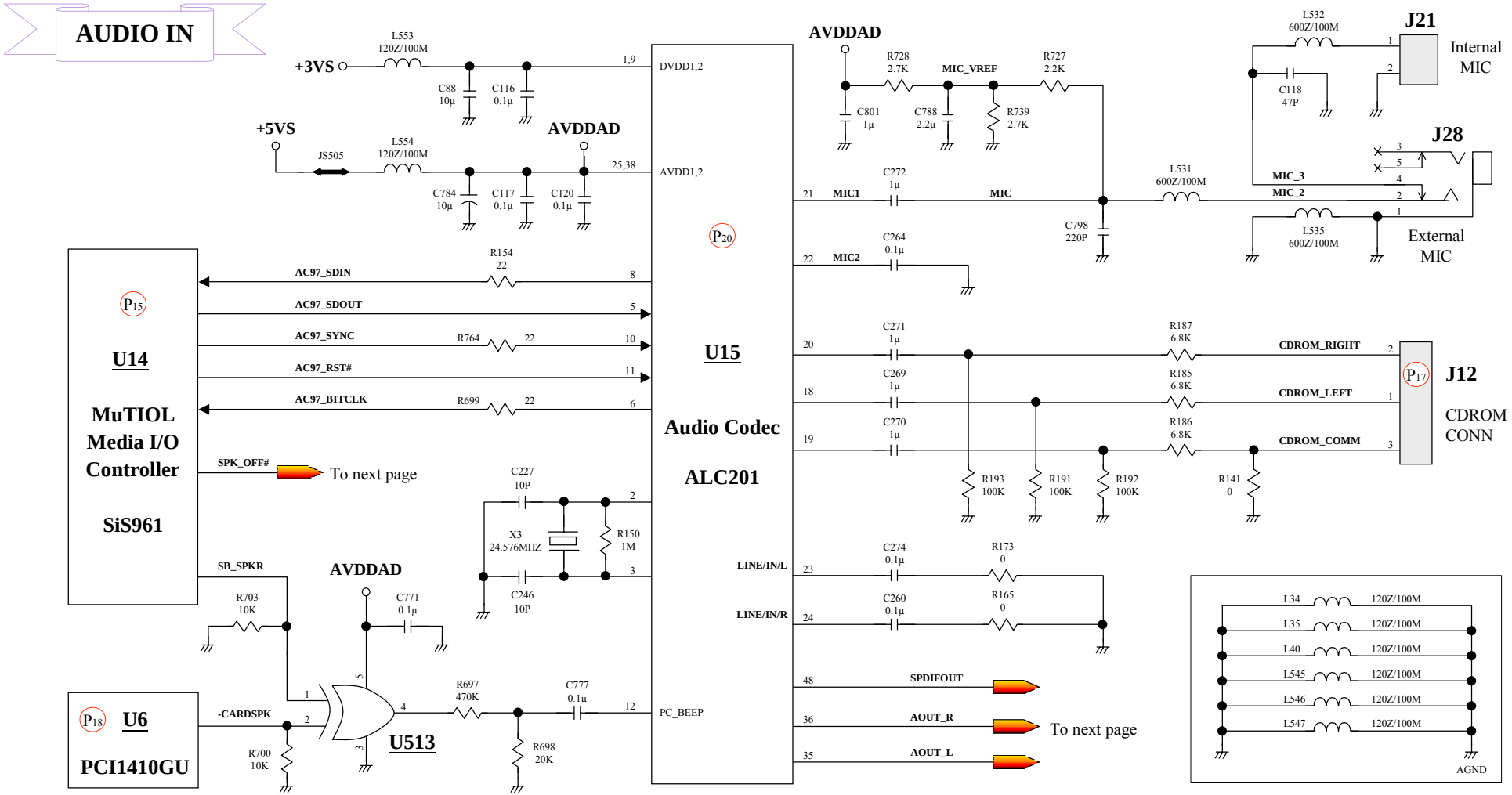
3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U14	CDROM_LEFT
U15	CDROM_RIGHT
J12	CDROM_COMM
R187	
R185	
R186	

8575 N/B Maintenance

8.11 Audio Failure

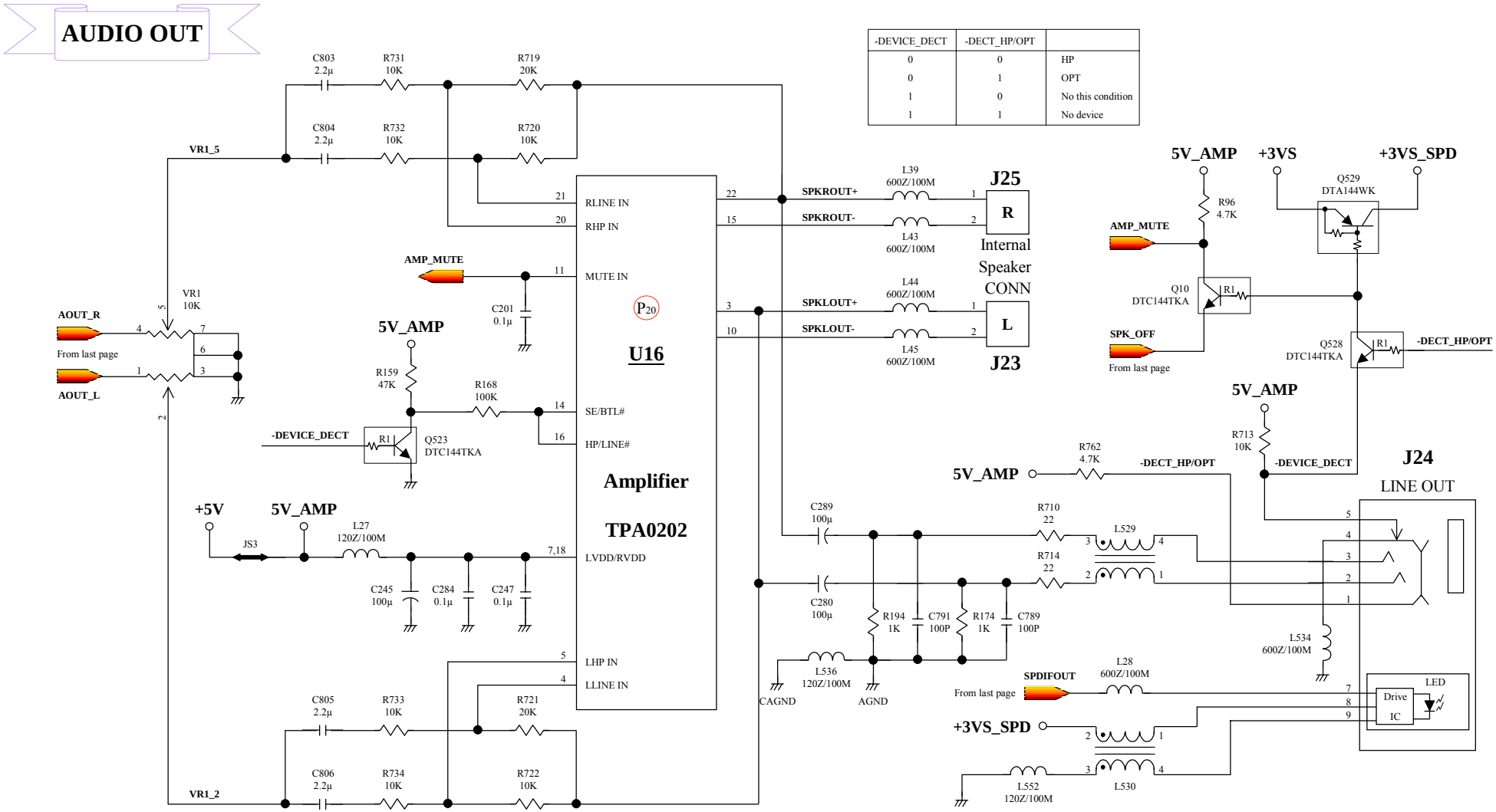
No sound from speaker after audio driver is installed.



8575 N/B Maintenance

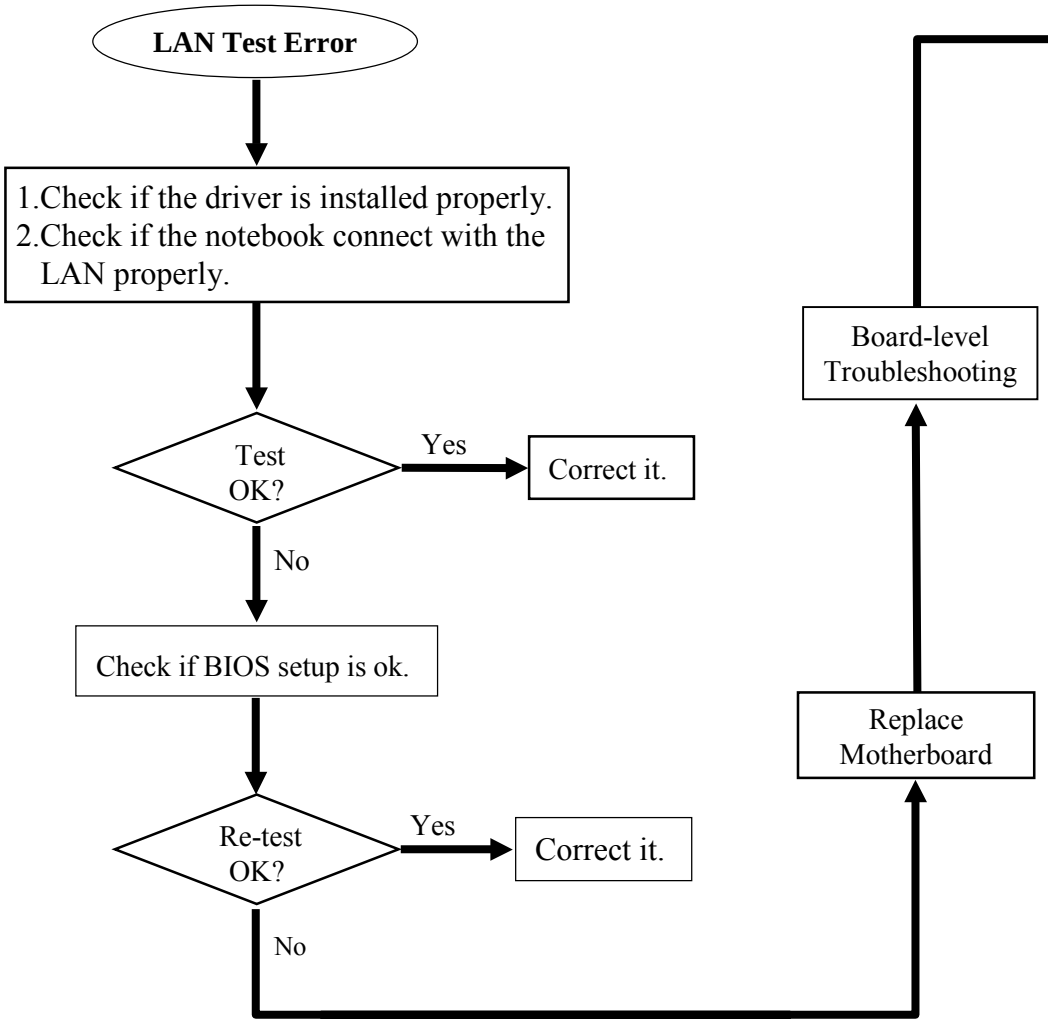
8.11 Audio Failure

No sound from speaker after audio driver is installed.



8.12 LAN Test Error

An error occurs when a LAN device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U14	RP6
U5	RP5
U3	X4
J9	L6
L5	L8
R171	R32
R177	L4
R166	R31
R167	R538
R172	R35
R178	R537
R72	X1
R69	
R67	

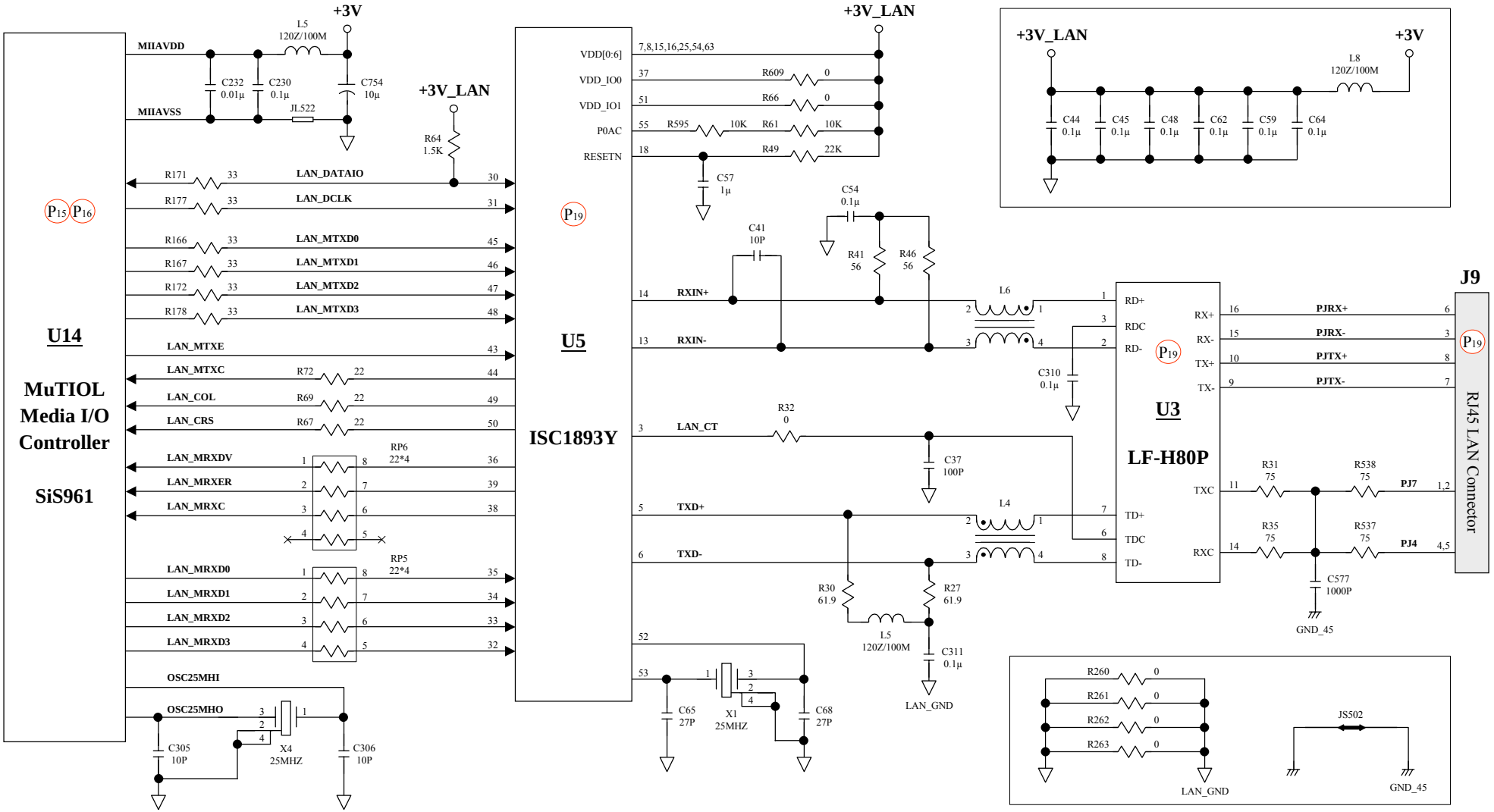
Signals:

MIIAVDD	RXIN+
+3V_LAN	RXIN-
LAN_DATAIO	LAN_CT
LAN_DCLK	TXD+
LAN_MTXD[0:3]	TXD-
LAN_MTXE	PJRX+
LAN_MTXC	PJRX-
LAN_COL	PJTX+
LAN_CRS	PJTX-
LAN_MRXDV	PJ8
LAN_MRXER	PJ7
LAN_MRXC	PJ5
LAN_MRXD[0:3]	PJ4
OSC25MHI	
OSC25MHO	

8575 N/B Maintenance

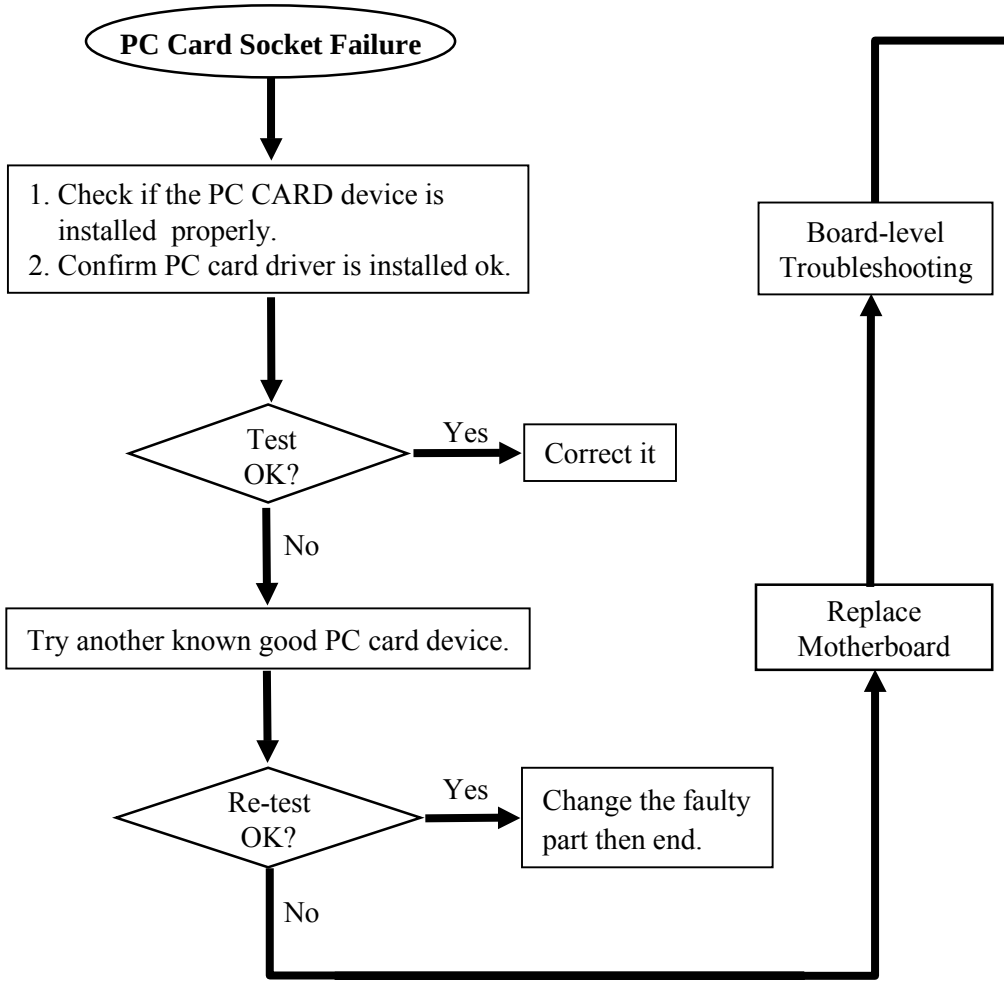
8.12 LAN Test Error

An error occurs when a LAN device is installed.



8.13 PC Card Socket Failure

An error occurs when a PC card device is installed.



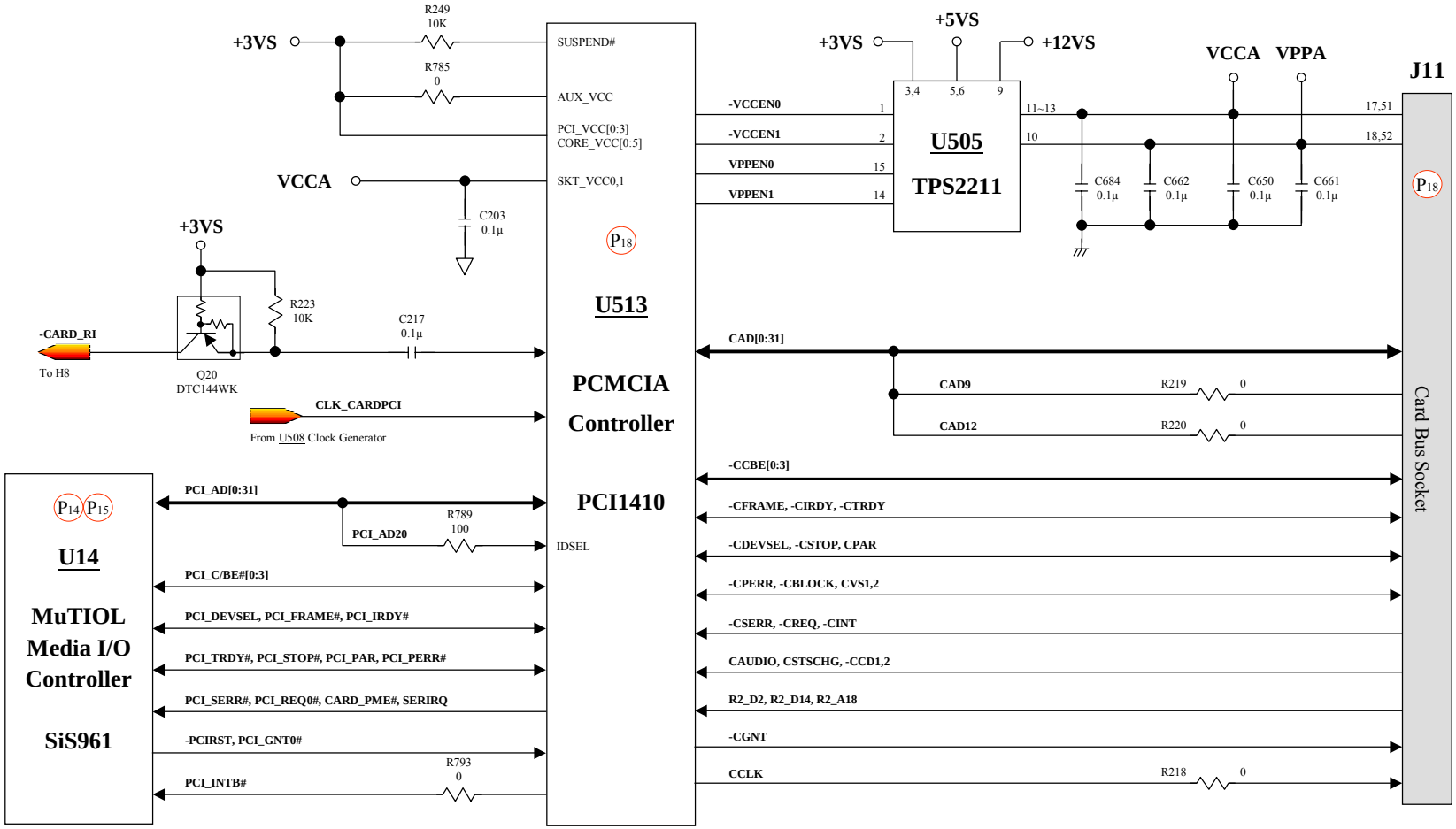
Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U14	PCI_AD[0:31]	PCI_SERR#
U508	PCI_C/BE# [0:3]	CARD_PME#
U513	PCI_REQ0#	SERIRQ
U505	PCI_FRAME#	-CARD_RI
J11	PCI_IRDY#	CLK_CARDPCI
R249	PCI_TRDY#	-VCCEN0
R785	PCI_DEVSEL#	-VCCEN1
Q20	PCI_STOP#	-VPPEN0
R789	PCI_INTC#	-VPPEN1
R793	-PCIRST#	+3VS
R219	PCI_GNT0#	VCCA
R220	PCI_PAR	VPPA
R218	PCI_PERR#	

8575 N/B Maintenance

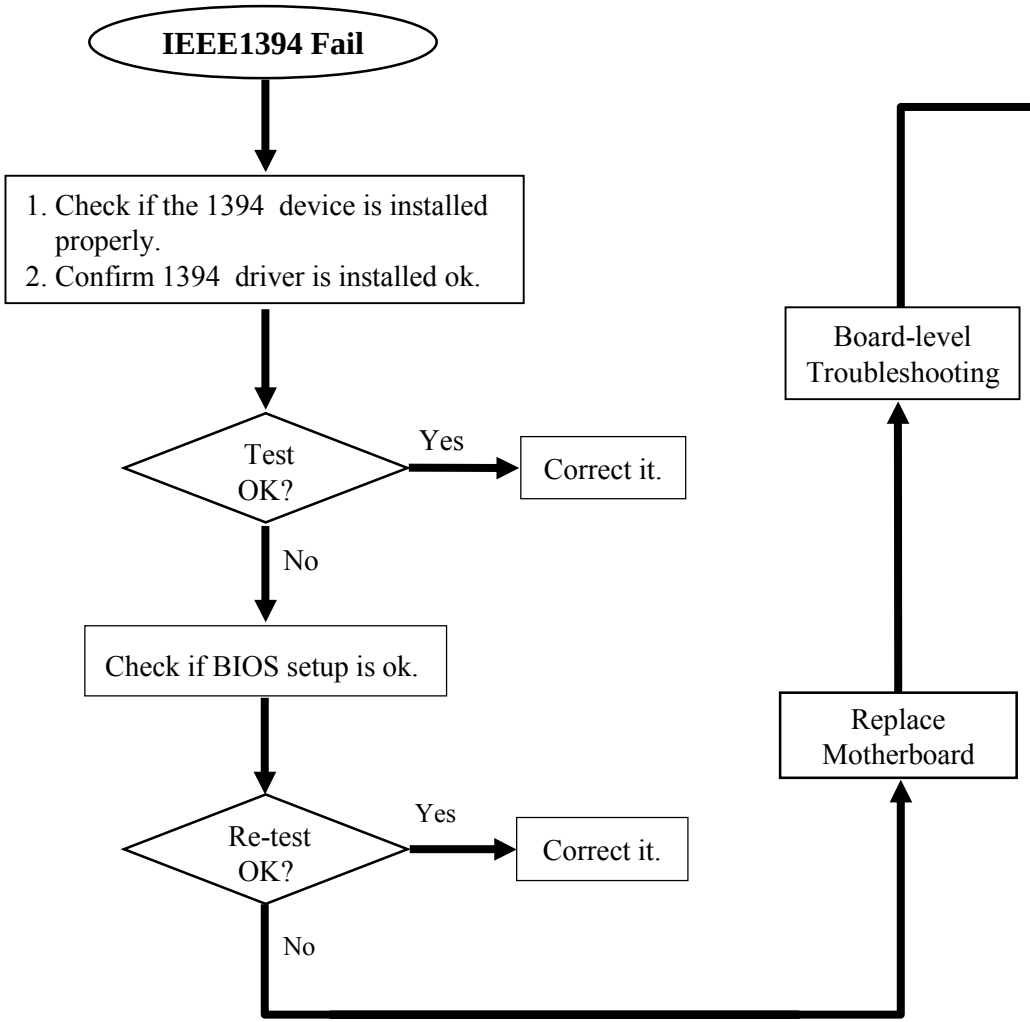
8.13 PC Card Socket Failure

An error occurs when a PC card device is installed.



8.14 IEEE 1394 Failure

An error occurs when a IEEE 1394 device is installed.



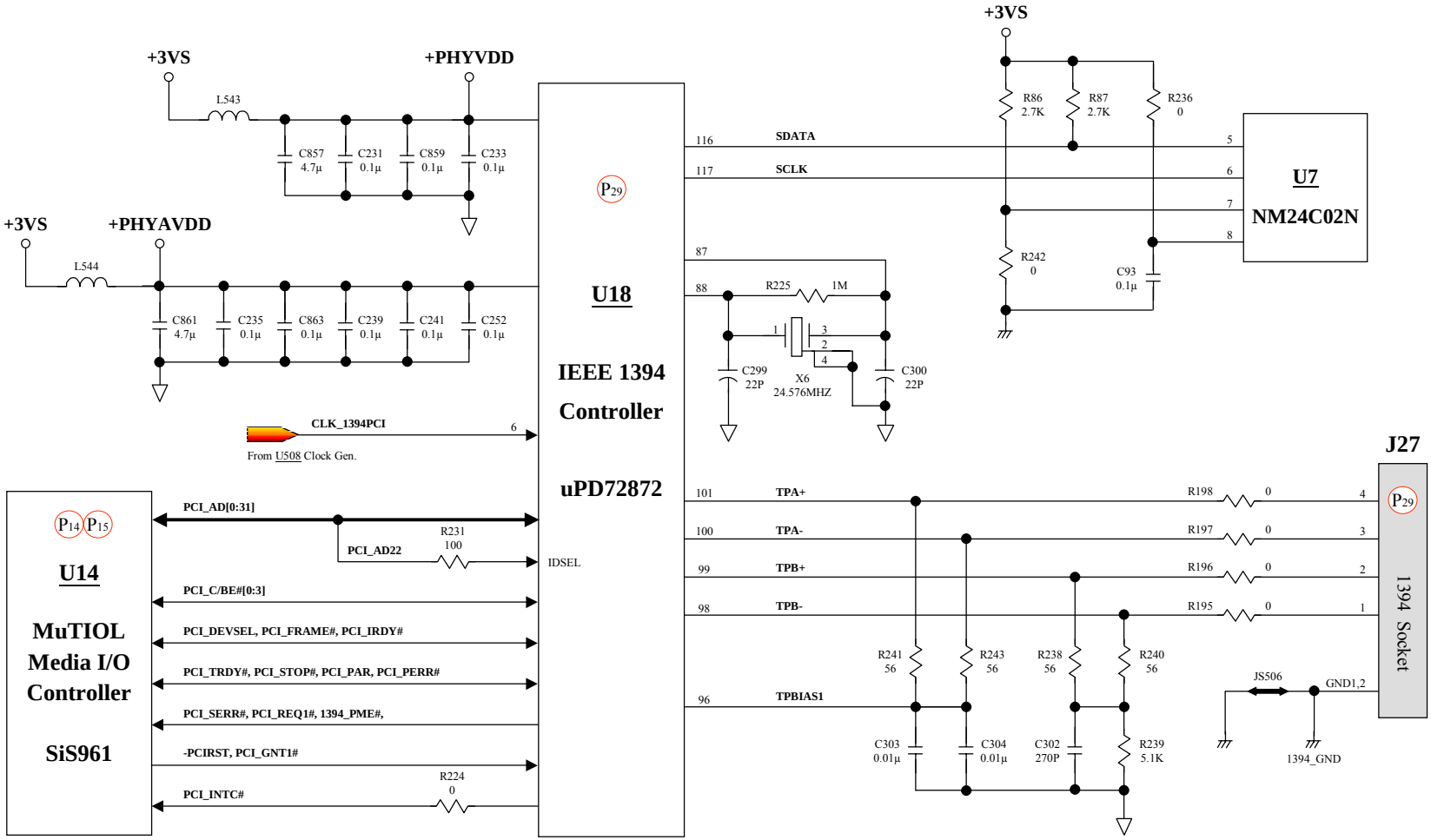
Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U14	PCI_AD[0:31]	PCI_SERR#
U508	PCI_C/BE# [0:3]	1394_PME#
U18	PCI_REQ1#	CLK_1394PCI
U7	PCI_FRAME#	SDATA
J27	PCI_IRDY#	SCLK
L543	PCI_TRDY#	TPA+
L544	PCI_DEVSEL#	TPA-
R231	PCI_STOP#	TPB+
R224	PCI_INTC#	TPB-
R198	-PCIRST#	TPBIAS1
R197	PCI_GNT1#	+3VS
R196	PCI_PAR	+PHYVDD
R195	PCI_PERR#	+PHYAVDD
R225		
X6		

8575 N/B Maintenance

8.14 IEEE 1394 Failure

An error occurs when a IEEE 1394 device is installed.



8575 N/B Maintenance

9. Spare Parts List - 1

8575 ID2 14”

Part Number	Description	Location(s)
541667170031	AK;EN,BOX,8575,UTILITY ONLY	
343671600014	AL-FOIL;HST-PANEL_15"-XGA,8175	
441999900057	BATT ASSY OPTION;LI,9-CELL,8175	
442671600001	BATT ASSY;11.1V/6AH,LI,PANASONIC	
221669940001	BOX;AK,7170	
342671600007	BRACKET;LCD,14",8175	
342671600005	BRACKET;LCD,R,14",8175	
221669950008	CARD BOARD;FRAME,PALLET,7170	
221669950006	CARD BOARD;TOP,PALLET,7170	
221671220002	CARTON;NON-BRAND,MSL,8170	
431671710001	CASE KIT;ID2,8575	
451671600031	CD ROM ME KIT;8175	
340671600012	COVER ASSY;DIMM,8175	
340671600029	COVER ASSY;HDD,8175	
340671600034	COVER ASSY;LCD,14",ID1-2,8175	
340671710001	COVER ASSY;SILVER,8575	
344671600042	COVER;DUMMY,ID1-2,8175	
344671600046	COVER;HINGE,ID1-2,8175	
344671600043	DUMMY CARD;PCMCIA,8175	
227671600001	END CAP;14.1",8175	
451671600051	HDD ME KIT;8175	
340671600020	HINGE;L,14",8175	
340671600018	HINGE;R,14",8175	
340671700002	HOUSING ASSY;8575	
340671600039	HOUSING ASSY;CDROM,8175	

8575 ID2 14”

Part Number	Description	Location(s)
340671600035	HOUSING ASSY;LCD,14",ID-2,8175	
451671710001	HOUSING KIT;ID2,8575	
346671700021	INSULATOR;REAR,SCREW,8575	
340671700014	KEYBOARD COVER;ASSY-S,8575	
451671700032	LABEL KIT;N-B,8575	
242671700001	LABEL;AGENCY-GLOBAL,8575	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
441671710031	LCD ASSY;UNIPAC,XGA,14.1",ID2,85	
451671710052	LCD ME KIT;UNIPAC,XGA,14.1",ID2,	
413000020289	LCD;UB141X01,TFT,14.1",XGA,UNIPA	
416267171901	LT PF OPTION;XGA,14.1",ID2,8575	
416267171001	LT PF;UNIPAC,XGA,14.1",ID2,85753	
526267171002	LTXNX;8575/T4XX/XXX/XXXX/L8D3B	
461671600002	PACKING KIT;N-B,14.1",8175	
227671600003	PAD;LCD/KB,ANIT-STATIC,8175	
224670830002	PALLET;1250*1080*130,7521N	
221669950001	PARTITION;AK BOX,7170	
221671650008	PARTITION;AK BOX,TOP,8175	
221671650005	PARTITION;BATT,AK BOX,8175	
221671650006	PARTITION;FDD,AK BOK,BTM,8175	
221671650004	PARTITION;FDD,AK BOX,8175	
221671250003	PARTITION;PALLET,8170	
221671650007	PARTITION;SIDE,AK BOX,8175	
222668820001	PE BAG;ANTI-STATIC,170x270MM,ORC	

9. Spare Parts List - 2

8575 ID2 14”

Part Number	Description	Location(s)
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,t=1.1,	
421671600006	WIRE ASSY;LCD,UNIPAC,14",XGA,817	
	P/N:526267171002	

8575 ID2 15”

Part Number	Description	Location(s)
541667170001	AK;01-EN,BOX,8575	
441999900057	BATT ASSY OPTION;LI,9-CELL,8175	
442671600001	BATT ASSY;11.1V/6AH,LI,PANASONIC	
340671600026	BEZEL ASSY;DVD-ROM,QUANTA,8175	
221671640001	BOX;AK,8175	
342671600006	BRACKET;LCD,L,15",8175	
342671600004	BRACKET;LCD,R,15",8175	
221669950008	CARD BOARD;FRAME,PALLET,7170	
221669950006	CARD BOARD;TOP,PALLET,7170	
221671220002	CARTON;NON-BRAND,MSL,8170	
431671710001	CASE KIT;ID2,8575	
451671600031	CD ROM ME KIT;8175	
340671600012	COVER ASSY;DIMM,8175	
340671600029	COVER ASSY;HDD,8175	
340671600032	COVER ASSY;LCD,15",ID1-2,8175	
340671710001	COVER ASSY;SILVER,8575	
344671600042	COVER;DUMMY,ID1-2,8175	
344671600046	COVER;HINGE,ID1-2,8175	
323760000011	DDR SODIMM MODULE;256MB,77.10621	
344671600043	DUMMY CARD;PCMCIA,8175	
523430061901	DVD DRIVE;8X,SDR-081,H=12.7,QUAN	
523467160014	DVD ROM ASSY;8X,SDR-081,QUANTA,8	
227671600002	END CAP;15.1",8175	
523411442518	FD DRIVE;1.44M,3.5",D353FUE,MITS	
345671700006	GASKET;BRACKET LCD,8575	

9. Spare Parts List - 3

8575 ID2 15”

Part Number	Description	Location(s)
523401634007	HD DRIVE;30GB,2.5",IC25N030ATCS0	
523467170009	HDD ASSY;30G,2.5",9.5MM,8575	
523499990099	HDD DRIVE OPTION;30G,2.5",9.5MM,	
451671600051	HDD ME KIT;8175	
340671600019	HINGE;L,15",8175	
340671600017	HINGE;R,15",8175	
340671700002	HOUSING ASSY;8575	
340671600039	HOUSING ASSY;CDROM,8175	
340671700011	HOUSING ASSY;LCD,HANSTAR,SILVER,	
451671710001	HOUSING KIT;ID2,8575	
324180786126	IC;CPU,P4-WILLAMETTE,1.7G,U-FCPG	
346671700008	INSULATOR;CABLE LCD,8575	
346671700021	INSULATOR;REAR,SCREW,8575	
531099990128	KBD OPTION;86,US,8175	
531020237342	KBD;86,US,K000918I1,8175	
340671700014	KEYBOARD COVER;ASSY-S,8575	
451671700032	LABEL KIT;N-B,8575	
242671700001	LABEL;AGENCY-GLOBAL,8575	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
441671710035	LCD ASSY;HANNSTAR,XGA,15.1",ID2,	
451671710054	LCD ME KIT;HANNSTAR,XGA,15.1",ID	
413000020296	LCD;HSD150PX11-A,TFT,15",XGA,HAN	
416267171004	LT PF;HANNSTAR,XGA,15.1",ID2,857	
526267171001	LTXNT;8575/5RCI/30C/1US1/L9D3B/X	

8575 ID2 15”

Part Number	Description	Location(s)
561567176001	MANUAL KIT;EN,8575,N-B	
561567170001	MANUAL;USER'S,EN,8575,N-B	
461671600010	PACKING KIT;N-B,15",8175	
227671600003	PAD;LCD/KB,ANIT-STATIC,8175	
224670830002	PALLET;1250*1080*130,7521N	
221671650001	PARTITION;AK BOX,8175	
221671650008	PARTITION;AK BOX,TOP,8175	
221671650005	PARTITION;BATT,AK BOX,8175	
221671650006	PARTITION;FDD,AK BOK,BTM,8175	
221671650004	PARTITION;FDD,AK BOX,8175	
221671250003	PARTITION;PALLET,8170	
221671650007	PARTITION;SIDE,AK BOX,8175	
222668820001	PE BAG;ANTI-STATIC,170x270MM,ORC	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	
565180626001	S/W;CD*1,DVD,WIN-DVD,INTERVIDEO	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
370101714501	SPC-SCREW;M1.7L4.5,NIB,K-HEAD	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,t=1.1,	
421671600004	WIRE ASSY;LCD,HANN,15",XGA,8175	
	P/N: 526267171001	

9. Spare Parts List - 4

8575 ID3 14”

Part Number	Description	Location(s)
541667170004	AK;04-EU,BOX,8575	
343671600014	AL-FOIL;HST-PANEL_15"-XGA,8175	
441999900065	BATT ASSY OPTION;LI-ION,2000mAH	
442671700003	BATT ASSY;11.1V/6AH,LI,ID3,MSL,8	
221671640001	BOX;AK,8175	
342671600003	BRACKET;HDD,8175	
342671600007	BRACKET;LCD,14",8175	
342671600005	BRACKET;LCD,R,14",8175	
221671650011	CARTON;5 IN 1,8175	
431671720001	CASE KIT;ID3,8575	
451671720091	CD-ROM ME KIT;TEAC,ID3,8575	
340671720008	COVER ASSY;DIMM,ID3,8575	
340671720001	COVER ASSY;ID3,8575	
340671720004	COVER ASSY;KB,ID3,8575	
340671720010	COVER ASSY;LCD,14",ID3,8575	
344671720002	COVER;DUMMY,ID3,8575	
344671720013	COVER;HDD,ID3,8575	
344671720023	COVER;HINGE,ID3,8575	
344670500042	DUMMY CARD;PCMCIA,TETRA	
227671600005	END CAP;5 IN 1,LOWER,8175	
227671600004	END CAP;5 IN 1,UPPER,8175	
345671600018	GASKET;HEATSINK,K/B_PLATE,8175	
451671720071	HDD ME KIT;ID3,8575	
340671600020	HINGE;L,14",8175	
340671600018	HINGE;R,14",8175	

8575 ID3 14”

Part Number	Description	Location(s)
340671720011	HOUSING ASSY;CDROM,ID3,8575	
340671720007	HOUSING ASSY;ID3,8575	
340671720003	HOUSING ASSY;LCD,14",ID3,8575	
451671720001	HOUSING KIT;ID3,8575	
346671720002	INSULATOR;REAR,SCREW,ID3,8575	
451671720032	LABEL KIT;N-B,8575 ID3	
242671720002	LABEL;AGENCY-GLOBAL,ID3,8575	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
441671720031	LCD ASSY;UNIPAC,XGA,14.1",ID3,85	
451671720052	LCD ME KIT;UNIPAC,XGA,14.1",ID3,	
413000020289	LCD;UB141X01,TFT,14.1",XGA,UNIPA	
416267172901	LT PF OPTION;XGA,14.1",ID3,8575	
416267172001	LT PF;UNIPAC,XGA,14.1",ID3,8575	
526267172004	LTXNX;8575/T4XX/XXX/3XX9/L9I33/X	
561567176003	MANUAL KIT;EU,8575,N-B	
561567170001	MANUAL;USER'S,EN,8575,N-B	
561567170003	MANUAL;USER'S,EU,8575,N-B	
461671600018	PACKING KIT;N-B,5 IN 1,8175	
221671650001	PARTITION;AK BOX,8175	
221671650008	PARTITION;AK BOX,TOP,8175	
221671650005	PARTITION;BATT,AK BOX,8175	
221671650006	PARTITION;FDD,AK BOK,BTM,8175	
221671650004	PARTITION;FDD,AK BOX,8175	
221671650007	PARTITION;SIDE,AK BOX,8175	

9. Spare Parts List - 5

8575 ID3 14”

Part Number	Description	Location(s)
222668820001	PE BAG;ANTI-STATIC,170x270MM,ORC	
332810000034	PWR CORD;250V/2.5A,2P,BLK,EU,175	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,	
370102610805	SPC-SCREW;M2.6L8,K-HD,NIW/NLK	
370102010302	SPC-SCREW;M2L3,NIW,K-HD,736	
421671600006	WIRE ASSY;LCD,UNIPAC,14",XGA,817	
	P/N: 526267172004	

8575 ID3 15”

Part Number	Description	Location(s)
541667170004	AK;04-EU,BOX,8575	
346671600021	AL-FOIL;CONDUCTIVE,LCD-SAM_XGA,8	
441999900065	BATT ASSY OPTION;LI-ION,2000mAH	
442671700003	BATT ASSY;11.1V/6AH,LI,ID3,MSL,8	
221671640001	BOX;AK,8175	
342671600003	BRACKET;HDD,8175	
342671600006	BRACKET;LCD,L,15",8175	
342671600004	BRACKET;LCD,R,15",8175	
221671650011	CARTON;5 IN 1,8175	
431671720001	CASE KIT;ID3,8575	
451671720091	CD-ROM ME KIT;TEAC,ID3,8575	
340671720008	COVER ASSY;DIMM,ID3,8575	
340671720001	COVER ASSY;ID3,8575	
340671720004	COVER ASSY;KB,ID3,8575	
340671720009	COVER ASSY;LCD,15",ID3,8575	
344671720002	COVER;DUMMY,ID3,8575	
344671720013	COVER;HDD,ID3,8575	
344671720023	COVER;HINGE,ID3,8575	
344670500042	DUMMY CARD;PCMCIA,TETRA	
227671600005	END CAP;5 IN 1,LOWER,8175	
227671600004	END CAP;5 IN 1,UPPER,8175	
345671600018	GASKET;HEATSINK,K/B_PLATE,8175	
451671720071	HDD ME KIT;ID3,8575	
340671600019	HINGE;L,15",8175	
340671600017	HINGE;R,15",8175	

9. Spare Parts List - 6

8575 ID3 15”

Part Number	Description	Location(s)
340671720011	HOUSING ASSY;CDROM,ID3,8575	
340671720007	HOUSING ASSY;ID3,8575	
340671720002	HOUSING ASSY;LCD,15",ID3,8575	
451671720001	HOUSING KIT;ID3,8575	
346671720002	INSULATOR;REAR,SCREW,ID3,8575	
451671720032	LABEL KIT;N-B,8575 ID3	
242671720002	LABEL;AGENCY-GLOBAL,ID3,8575	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
441671720034	LCD ASSY;SAMSUNG,XGA,15.1",ID3,8	
451671720053	LCD ME KIT;SAMSUNG,XGA,15.1",ID3	
413000020265	LCD;LT150X3-124,TFT,15",LVDS,XGA	
416267172902	LT PF OPTION;XGA,15",ID3,8575	
416267172003	LT PF;SAMSUNG,XGA,15.1",ID3,8575	
526267172003	LTXNX;8575/T5XX/XXX/3XX9/L9I33/X	
561567176003	MANUAL KIT;EU,8575,N-B	
561567170001	MANUAL;USER'S,EN,8575,N-B	
561567170003	MANUAL;USER'S,EU,8575,N-B	
461671600018	PACKING KIT;N-B,5 IN 1,8175	
221671650001	PARTITION;AK BOX,8175	
221671650008	PARTITION;AK BOX,TOP,8175	
221671650005	PARTITION;BATT,AK BOX,8175	
221671650006	PARTITION;FDD,AK BOK,BTM,8175	
221671650004	PARTITION;FDD,AK BOX,8175	
221671650007	PARTITION;SIDE,AK BOX,8175	

8575 ID3 15”

Part Number	Description	Location(s)
222668820001	PE BAG;ANTI-STATIC,170x270MM,ORC	
332810000034	PWR CORD;250V/2.5A,2P,BLK,EU,175	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,	
370102610805	SPC-SCREW;M2.6L8,K-HD,NIW/NLK	
370102010302	SPC-SCREW;M2L3,NIW,K-HD,736	
421671600002	WIRE ASSY;LCD,SAM,15",XGA,8175	
	P/N: 526267172003	

9. Spare Parts List - 7

8575 ID4 14”

Part Number	Description	Location(s)
541667170001	AK;01-EN,BOX,8575	
441999900062	BATT ASSY OPTION;LI,9-CELL,8575	
442671700002	BATT ASSY;11.1V/6AH,LI,MSL,8575	
340671600026	BEZEL ASSY;DVD-ROM,QUANTA,8175	
221671640001	BOX;AK,8175	
342671600007	BRACKET;LCD,14",8175	
342671600005	BRACKET;LCD,R,14",8175	
221669950008	CARD BOARD;FRAME,PALLET,7170	
221669950006	CARD BOARD;TOP,PALLET,7170	
221671220002	CARTON;NON-BRAND,MSL,8170	
431671700001	CASE KIT;8575	
451671600031	CD ROM ME KIT;8175	
340671700001	COVER ASSY;8575	
340671600012	COVER ASSY;DIMM,8175	
340671600029	COVER ASSY;HDD,8175	
340671600022	COVER ASSY;LCD,14",8175	
344671600010	COVER;DUMMY,8175	
344671600011	COVER;HINGE,8175	
323760000011	DDR SODIMM MODULE;256MB,77.10621	
344671600043	DUMMY CARD;PCMCIA,8175	
523430061901	DVD DRIVE;8X,SDR-081,H=12.7,QUAN	
523467160014	DVD ROM ASSY;8X,SDR-081,QUANTA,8	
227671600001	END CAP;14.1",8175	
523411442518	FD DRIVE;1.44M,3.5",D353FUE,MITS	
345671600018	GASKET;HEATSINK,K/B_PLATE,8175	

8575 ID4 14”

Part Number	Description	Location(s)
523401634007	HD DRIVE;30GB,2.5",IC25N030ATCS0	
523467170009	HDD ASSY;30G,2.5",9.5MM,8575	
523499990099	HDD DRIVE OPTION;30G,2.5",9.5MM,	
451671600051	HDD ME KIT;8175	
340671600020	HINGE;L,14",8175	
340671600018	HINGE;R,14",8175	
340671700002	HOUSING ASSY;8575	
340671600039	HOUSING ASSY;CDROM,8175	
340671730002	HOUSING ASSY;LCD,14",ID4,8575	
451671700001	HOUSING KIT;8575	
324180786126	IC;CPU,P4-WILLAMETTE,1.7G,U-FCPG	
346671700021	INSULATOR;REAR,SCREW,8575	
531099990128	KBD OPTION;86,US,8175	
531020237342	KBD;86,US,K000918I1,8175	
340671700015	KEYBOARD COVER;ASSY-B,8575	
451671700032	LABEL KIT;N-B,8575	
242671700001	LABEL;AGENCY-GLOBAL,8575	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
441671730005	LCD ASSY;QDI,XGA,14.1",ID4,8575	
451671730005	LCD ME KIT;QDI,XGA,14.1",ID4,857	
413000020304	LCD;QD141X1LH03,TFT,14.1",LCDS,X	
416267173006	LT PF;QDI,XGA,14.1",ID4,8575	
526267173009	LTXNT;8575/4QCI/30C/1US1/L9D3D/X	
561567176001	MANUAL KIT;EN,8575,N-B	

8575 N/B Maintenance

9. Spare Parts List - 8

8575 ID4 14”

Part Number	Description	Location(s)
561567170001	MANUAL;USER'S,EN,8575,N-B	
461671600002	PACKING KIT;N-B,14.1",8175	
227671600003	PAD;LCD/KB,ANIT-STATIC,8175	
224670830002	PALLET;1250*1080*130,7521N	
221671650001	PARTITION;AK BOX,8175	
221671650008	PARTITION;AK BOX,TOP,8175	
221671650005	PARTITION;BATT,AK BOX,8175	
221671650006	PARTITION;FDD,AK BOK,BTM,8175	
221671650004	PARTITION;FDD,AK BOX,8175	
221671250003	PARTITION;PALLET,8170	
221671650007	PARTITION;SIDE,AK BOX,8175	
222668820001	PE BAG;ANTI-STATIC,170x270MM,ORC	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	
565180626001	S/W;CD*1,DVD,WIN-DVD,INTERVIDEO	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
370101714501	SPC-SCREW;M1.7L4.5,NIB,K-HEAD	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,t=1.1,	
421671600006	WIRE ASSY;LCD,UNIPAC,14",XGA,817	
	P/N: 526267173009	

8575 ID4 15”

Part Number	Description	Location(s)
541667170004	AK;04-EU,BOX,8575	
346671600021	AL-FOIL;CONDUCTIVE,LCD-SAM_XGA,8	
441999900062	BATT ASSY OPTION;LI,9-CELL,8575	
442671700002	BATT ASSY;11.1V/6AH,LI,MSL,8575	
221671640001	BOX;AK,8175	
342671600006	BRACKET;LCD,L,15",8175	
342671600004	BRACKET;LCD,R,15",8175	
221671650011	CARTON;5 IN 1,8175	
431671700001	CASE KIT;8575	
451671600031	CD ROM ME KIT;8175	
340671700001	COVER ASSY;8575	
340671600012	COVER ASSY;DIMM,8175	
340671600029	COVER ASSY;HDD,8175	
340671600021	COVER ASSY;LCD,15",8175	
344671600010	COVER;DUMMY,8175	
344671600011	COVER;HINGE,8175	
344671600043	DUMMY CARD;PCMCIA,8175	
227671600005	END CAP;5 IN 1,LOWER,8175	
227671600004	END CAP;5 IN 1,UPPER,8175	
345671600018	GASKET;HEATSINK,K/B_PLATE,8175	
451671600051	HDD ME KIT;8175	
340671600019	HINGE;L,15",8175	
340671600017	HINGE;R,15",8175	
340671700002	HOUSING ASSY;8575	
340671600039	HOUSING ASSY;CDROM,8175	

9. Spare Parts List - 9

8575 ID4 15”

Part Number	Description	Location(s)
340671730001	HOUSING ASSY;LCD,15",ID4,8575	
451671700001	HOUSING KIT;8575	
346671700021	INSULATOR;REAR,SCREW,8575	
340671700015	KEYBOARD COVER;ASSY-B,8575	
451671700032	LABEL KIT;N-B,8575	
242671700001	LABEL;AGENCY-GLOBAL,8575	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
441671730001	LCD ASSY;SAMSUNG,XGA,15”,ID4,85	
451671730001	LCD ME KIT;SAMSUNG,XGA,15”,ID4,	
413000020265	LCD;LT150X3-124,TFT,15",LVDS,XGA	
416267173003	LT PF;SAMSUNG,XGA,15.1",ID4,8575	
526267173005	LTXNX;8575/T5XX/XXX/3XX9/L9I3D/X	
561567176003	MANUAL KIT;EU,8575,N-B	
561567170001	MANUAL;USER'S,EN,8575,N-B	
561567170003	MANUAL;USER'S,EU,8575,N-B	
416267173902	NB PF OPTION;XGA,15",ID4,8575	
461671600018	PACKING KIT;N-B,5 IN 1,8175	
221671650001	PARTITION;AK BOX,8175	
221671650008	PARTITION;AK BOX,TOP,8175	
221671650005	PARTITION;BATT,AK BOX,8175	
221671650006	PARTITION;FDD,AK BOK,BTM,8175	
221671650004	PARTITION;FDD,AK BOX,8175	
221671650007	PARTITION;SIDE,AK BOX,8175	
222668820001	PE BAG;ANTI-STATIC,170x270MM,ORC	

8575 ID4 15”

Part Number	Description	Location(s)
332810000034	PWR CORD;250V/2.5A,2P,BLK,EU,175	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,t=1.1,	
421671600002	WIRE ASSY;LCD,SAM,15",XGA,8175	
	P/N: 526267173005	

9. Spare Parts List - 10

8575 ID5 14”

Part Number	Description	Location(s)
541667170001	AK;01-EN,BOX,8575	
343671600014	AL-FOIL;HST-PANEL_15"-XGA,8175	
441999900062	BATT ASSY OPTION;LI,9-CELL,8575	
442671700002	BATT ASSY;11.1V/6AH,LI,MSL,8575	
340671600026	BEZEL ASSY;DVD-ROM,QUANTA,8175	
221671640001	BOX;AK,8175	
342671600007	BRACKET;LCD,14",8175	
342671600005	BRACKET;LCD,R,14",8175	
221669950008	CARD BOARD;FRAME,PALLET,7170	
221669950006	CARD BOARD;TOP,PALLET,7170	
221671220002	CARTON;NON-BRAND,MSL,8170	
431671710001	CASE KIT;ID2,8575	
451671600031	CD ROM ME KIT;8175	
340671600012	COVER ASSY;DIMM,8175	
340671600029	COVER ASSY;HDD,8175	
340671600034	COVER ASSY;LCD,14",ID1-2,8175	
340671710001	COVER ASSY;SILVER,8575	
344671600042	COVER;DUMMY,ID1-2,8175	
344671600046	COVER;HINGE,ID1-2,8175	
323760000011	DDR SODIMM MODULE;256MB,77.10621	
344671600043	DUMMY CARD;PCMCIA,8175	
523430061901	DVD DRIVE;8X,SDR-081,H=12.7,QUAN	
523467160014	DVD ROM ASSY;8X,SDR-081,QUANTA,8	
227671600001	END CAP;14.1",8175	
523411442518	FD DRIVE;1.44M,3.5",D353FUE,MITS	

8575 ID5 14”

Part Number	Description	Location(s)
523401634007	HD DRIVE;30GB,2.5",IC25N030ATCS0	
523467170009	HDD ASSY;30G,2.5",9.5MM,8575	
523499990099	HDD DRIVE OPTION;30G,2.5",9.5MM,	
451671600051	HDD ME KIT;8175	
340671600020	HINGE;L,14",8175	
340671600018	HINGE;R,14",8175	
340671700002	HOUSING ASSY;8575	
340671600039	HOUSING ASSY;CDROM,8175	
340671740002	HOUSING ASSY;LCD,14",ID5,8575	
451671710001	HOUSING KIT;ID2,8575	
324180786126	IC;CPU,P4-WILLAMETTE,1.7G,U-FCPG	
346671700021	INSULATOR;REAR,SCREW,8575	
531099990128	KBD OPTION;86,US,8175	
531020237342	KBD;86,US,K000918I1,8175	
340671700014	KEYBOARD COVER;ASSY-S,8575	
451671700032	LABEL KIT;N-B,8575	
242671700001	LABEL;AGENCY-GLOBAL,8575	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
441671740005	LCD ASSY;QDI,XGA,14.1",ID5,8575	
451671740005	LCD ME KIT;QDI,XGA,14.1",ID5,857	
413000020304	LCD;QD141X1LH03,TFT,14.1",LCDS,X	
416267174006	LT PF;QDI,XGA,14.1",ID5,8575	
526267174007	LTXNT;8575/4QCI/30C/1US1/L9D3E/X	
561567170001	MANUAL;USER'S,EN,8575,N-B	

9. Spare Parts List - 11

8575 ID5 14”

Part Number	Description	Location(s)
461671600002	PACKING KIT;N-B,14.1",8175	
227671600003	PAD;LCD/KB,ANIT-STATIC,8175	
224670830002	PALLET;1250*1080*130,7521N	
221671650001	PARTITION;AK BOX,8175	
221671650008	PARTITION;AK BOX,TOP,8175	
221671650005	PARTITION;BATT,AK BOX,8175	
221671650006	PARTITION;FDD,AK BOK,BTM,8175	
221671650004	PARTITION;FDD,AK BOX,8175	
221671250003	PARTITION;PALLET,8170	
221671650007	PARTITION;SIDE,AK BOX,8175	
222668820001	PE BAG;ANTI-STATIC,170x270MM,ORC	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	
565180626001	S/W;CD*1,DVD,WIN-DVD,INTERVIDEO	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
370101714501	SPC-SCREW;M1.7L4.5,NIB,K-HEAD	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,t=1.1,	
421671600006	WIRE ASSY;LCD,UNIPAC,14",XGA,817	
	P/N: 526267174007	

8575 ID5 15”

Part Number	Description	Location(s)
541667170002	AK;02-EN,BAG,8575	
346671600021	AL-FOIL;CONDUCTIVE,LCD-SAM_XGA,8	
441999900062	BATT ASSY OPTION;LI,9-CELL,8575	
442671700002	BATT ASSY;11.1V/6AH,LI,MSL,8575	
342671600006	BRACKET;LCD,L,15",8175	
342671600004	BRACKET;LCD,R,15",8175	
221669950008	CARD BOARD;FRAME,PALLET,7170	
221669950006	CARD BOARD;TOP,PALLET,7170	
220671600002	CARRY BAG;N-B,8175	
221671220002	CARTON;NON-BRAND,MSL,8170	
431671710001	CASE KIT;ID2,8575	
451671600031	CD ROM ME KIT;8175	
340671600012	COVER ASSY;DIMM,8175	
340671600029	COVER ASSY;HDD,8175	
340671600032	COVER ASSY;LCD,15",ID1-2,8175	
340671710001	COVER ASSY;SILVER,8575	
344671600042	COVER;DUMMY,ID1-2,8175	
344671600046	COVER;HINGE,ID1-2,8175	
344671600043	DUMMY CARD;PCMCIA,8175	
523499995047	DVD COMBO ASSY OPTION;8175	
523467170003	DVD-COMBO ASSY;UJDA720MT-B,8575	
523408619025	DVD-COMBO DRIVE;UJDA720,8175	
227671600002	END CAP;15.1",8175	
227669900007	END CAP;IN BAG,7170	
451671600051	HDD ME KIT;8175	

9. Spare Parts List - 12

8575 ID5 15”

Part Number	Description	Location(s)
340671600019	HINGE;L,15",8175	
340671600017	HINGE;R,15",8175	
340671700002	HOUSING ASSY;8575	
340671600039	HOUSING ASSY;CDROM,8175	
340671740001	HOUSING ASSY;LCD 15",ID5,8575	
451671710001	HOUSING KIT;ID2,8575	
346671700021	INSULATOR;REAR,SCREW,8575	
531099990133	KBD OPTION;87,FR,8175	
531020237350	KBD;87,FR,K000918J1,8175	
340671700014	KEYBOARD COVER;ASSY-S,8575	
451671700032	LABEL KIT;N-B,8575	
242671700001	LABEL;AGENCY-GLOBAL,8575	
242600000157	LABEL;BAR CODE,125*65,COMMON	
441671740001	LCD ASSY;SAMSUNG,XGA,15.1",ID5,8	
451671740001	LCD ME KIT;SAMSUNG,XGA,15.1",ID5	
413000020265	LCD;LT150X3-124,TFT,15",LVDS,XGA	
416267174003	LT PF;SAMSUNG,XGA,15.1",ID5,8575	
526267174002	LTXNX;8575/T5XX/XXK/3FR9/L9C3E/X	
561567170001	MANUAL;USER'S,EN,8575,N-B	
416267174902	NB PF OPTION;XGA,15",ID5,8575	
461671600012	PACKING KIT;N-B,BAG,15",8175	
227671600003	PAD;LCD/KB,ANIT-STATIC,8175	
224670830002	PALLET;1250*1080*130,7521N	
221671250002	PARTITION;CARRY BAG,8170	
221671250001	PARTITION;IN BAG,8170	

8575 ID5 15”

Part Number	Description	Location(s)
221671250003	PARTITION;PALLET,8170	
222668820004	PE BUBBLE BAG;190X190MM,ANTI-STA	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	
565180626001	S/W;CD*1,DVD,WIN-DVD,INTERVIDEO	
565167000013	S/W;CD-ROM,B'S RECORDER GOLD2.0	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,t=1.1,	
421671600002	WIRE ASSY;LCD,SAM,15",XGA,8175	
	P/N: 526267174002	

9. Spare Parts List - 13

8575-ID2/ID3/ID4/ID5 Common Spare Parts

Part Number	Description	Location(s)
441999900205	AC ADPT ASSY OPTION;8575	
442671200004	AC ADPT ASSY;19V/4.74A,DELTA,817	
541667170032	AK;EN,8575,UTILITY ONLY	
346671700016	AL-FOIL;HDD,M/B,8575	
242670800113	BFM-WORLD MARK;WINXP,7521N	
340671600028	BRACKET ASSY;T/P,INSULATOR,8175	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
272072153401	CAP;.015U ,CR,16V,10%,0603,X7R,S	C152,C154,C172,C192
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C212,C213,C232,C26,C265,C
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC16,PC20,PC27,PC541
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC525,PC551
272005103401	CAP;.01U ,CR,50V,10%,0805,X7R	PC519
272005103401	CAP;.01U ,CR,50V,10%,0805,X7R	PC501,PC583
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,S	PC10
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	C143,C144,C145,C146,C147,
272073104701	CAP;.1U ,25V,+80-20%,0603,Y5V,S	PC4,PC502
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C504,C506,C512,C513,C517,
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C106,C107,C108,C110,C111,
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	PC542,PC572
272003104701	CAP;.1U ,CR,25V ,+80-20%,0805,Y	C803,C805,PC22,PC23,PC25,
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	C101,C130,C151,C153,C155,
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C501,C502,C577
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	C1,C11,C534,C9,PC13,PC23,
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	PC28,PC29,PC521,PC527,PC
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,S	PC22

Part Number	Description	Location(s)
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C4,C7
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C1,C122,C126,C37,C579,C78
272075100701	CAP;10P ,50V ,+-10%,0603,NPO,SM	C196,C227,C246,C41,C43,C7
272075100302	CAP;10P ,CR,50V ,5%,0603,NPO,SM	C701,C702
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	PC31
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	C100,C132,C133
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C10,C12,C14,C15,C16,C18,C
272012106701	CAP;10U ,16V ,+80-20%,1206,Y5U,	C531,PC21
272012106701	CAP;10U ,16V ,+80-20%,1206,Y5U,	C698,PC24,PC27,PC533,PC5
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,S	PC1,PC2
272023106501	CAP;10U ,25V ,20%,1210,Y5U,SMT	PC546,PC577
272073151301	CAP;150P ,CR,25V,5% ,0603,NPO,SM	PC9
272073151301	CAP;150P ,CR,25V,5% ,0603,NPO,SM	PC573
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	PC12,PC30
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	C17,C9,PC524,PC531,PC547,
272431157508	CAP;150U ,UE,6.3V ,20%,7343,SP-C	PC29
272075150301	CAP;15P ,CR,50V ,5% ,0603,NPO,S	C291
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C10,C3,C509,C8
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C136,C137,C138,C139,C140,
272001105402	CAP;1U ,CR,10V,10%,0805,X5R,SM	PC5
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC550
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5	C521,C546,PC566
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C283,C788,C804,C806
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C522
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C714

9. Spare Parts List - 14

Part Number	Description	Location(s)
272075200302	CAP;20P ,CR,50V ,5% ,0603,SMT	C290
272075222701	CAP;2200P,50V ,+/-20%,0603,X7R,S	C23,PC548,PC562
272075221302	CAP;220P ,50V ,5% ,0603,NPO,SMT	PC18,PC28
272075221302	CAP;220P ,50V ,5% ,0603,NPO,SMT	C519,C520,C549,C550,C798
272431227504	CAP;220U ,4V ,20%,7343,POSCAP,SM	PC20
272075220701	CAP;22P ,50V ,+ -10%,0603,NPO,S	C121,C125,C299,C300,C504,
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C610,C651
272021226701	CAP;22U ,10V,+80-20%,1210,Y5V,S	C109,C11,C21,C22,C255,C51
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C2,C5
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C302,C38,C81
272075270302	CAP;27P ,50V ,5%,0603,COG,SMT	C65,C68
272075330401	CAP;33P ,CR,50V ,10%,0603,X7R,S	C12,C13
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C756,C857,C861
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C273,C648,C699
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	PC19
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	PC534,PC536,PC541,PC556,
272075470701	CAP;47P ,50V ,+ -10%,0603,NPO,S	C118,C222,C228
272431476502	CAP;47U ,6.3V,20%,SP-CON,7343,S	PC11
272075680302	CAP;68P ,50V ,5% ,0603,NPO,SMT	C707,C710
313000020360	CHOKE COIL;1.25uH,+30-0%,4.5Ts,D	PL1,PL2
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L508,L509,L518,L522
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L1,L4,L529,L530,L6
331000008038	CON;BAT,8P,2.5MM,SUYIN	J14
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J2
331720025005	CON;D,FM,25P,2.775,R/A	J3

Part Number	Description	Location(s)
291000153006	CON;FPC/FFC,15P*2,.8MM,BD/BD,ST,	J18
291000144004	CON;FPC/FFC,20P*2,1.0MM,H=4.6,ST	J3
291000142404	CON;FPC/FFC,24P,1MM,H8.2,ST,ACES	J13
291000150804	CON;FPC/FFC,8P,1MM,R/A,2CONTAC,E	J501
331040020004	CON;HDR,FM,10P*2,2.54MM,R/A,H8,4	J4
331030044013	CON;HDR,FM,22*2,2MM,ST,C16805	
331040050013	CON;HDR,FM,25P*2,1.27X1.27MM,D/R	J7
291000011024	CON;HDR,FM,5P*2,1.27MM,ST,H4.5,S	J501
331040020005	CON;HDR,MA,10P*2,2.54MM,R/A,H8.4	PJ1
291000011209	CON;HDR,MA,12P*1,1.25,ST,SMT	J6
291000024409	CON;HDR,MA,22P*2,2MM,R/A,SMT,ALL	J19
331040050012	CON;HDR,MA,25P*2,1.27X1.27MM,D/R	PJ2
291000020202	CON;HDR,MA,2P*1,1.25,R/A,SMT,HIR	J508
331040050010	CON;HDR,MA,50P,0.8MM,R/A,H1.1	J12
291000011030	CON;HDR,MA,5P*2,1.27MM,ST,H17,85	J6
291000020303	CON;HDR,SHROUD,MA,3P,1.25MM,R/A,	J503
291000256823	CON;IC CARD PART;68P,0.635,H5,SM	J11
331000004018	CON;IEEE1394,MA,4P,.8MM,R/A,LINK	J27
331870004017	CON;MINI DIN,4P,R/A,W/GROND,C108	J1
331870004010	CON;MINI DIN,4P,R/A,W/GROUND,C10	
291000810205	CON;PHONE JACK,2P,H=8.4,R/A,SMT	J1
291000810802	CON;PHONE JACK,8P,H=12.59,R/A,RJ	J9
331840010005	CON;POF MINI JACK,10P,W/SPDIF,2F	J24
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	J2
331840005013	CON;STEREO JACK,5P,R/A,28MF60-07	J28

9. Spare Parts List - 15

Part Number	Description	Location(s)
331000004029	CON;USB,MA,R/A,4P*1,2551A-04G5T-	J4,J5,J7,J8
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J21,J23,J25,J5
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J8
291000410401	CON;WFR,MA,4P,1.25MM,ST,SMT	J502
291000410801	CON;WFR,MA,8P*1,1.25MM,ST,SMT	J20
313000150093	CORE;LAN CORE,230OHM/100MHZ,LF-1	
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP501,CP502,CP503,CP504,(
331660020003	DIMM SOCKET;DDR SODIMM 200P,AMP1	J506
331660020002	DIMM SOCKET;DDR SODIMM200P,AMP13	J505
288110355001	DIODE;1SS355,80V,100mA,SOD-23,SM	PD503
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D501,PD2,PD3,PD515,PD51(
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD506,PD507,PD510,PD7
288100054001	DIODE;BAT54,30V,200mA,SOT-23	D509,D510
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D511
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1,D3,D4,D6
288100099001	DIODE;BAV99,70V,450MA,SOT-23	PD5,PD8
288100056003	DIODE;BAW56,70V,215MA,SOT-23	D3,D504
288100056003	DIODE;BAW56,70V,215MA,SOT-23	D514
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD1,PD4
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD1,PD2
288100112001	DIODE;EC11FS2,1A,FAST RECOVERY,S	PD503,PD504,PD511
288100112003	DIODE;EC11FS2-TE12L,SCHOTTKY,200	PD504,PD505
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD505,PD506,PD514
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD3,PD4,PD501,PD502,PD5
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D11,D14,D15,D16,D17,D513

Part Number	Description	Location(s)
288100020001	DIODE;RLZ20C,ZENER,19.23V,5%,SMT	PD511
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD501
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	D10,D5,D508
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	D516
272601107501	EC;100U ,6.3V,20%,D6.3,-40+85'C,	C280,C289
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C245
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC25
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC15,PC17,PC18
312271005357	EC;10U,25V,20%,RA,6.3*6.8,+105℃	PC2,PC3
312271005357	EC;10U,25V,20%,RA,6.3*6.8,+105℃	PC11,PC12,PC14
312273361501	EC;330U ,6.3V ,RA,M,6.3*7,+105C	PC1,PC6
312304705351	EC;47U,25V,20%,D10X10.5,105'C,SY	PC31,PC32,PC33
312278206152	EC;820U ,4V,+-20%,10X10.5,FPCAP	PC3,PC5,PC7,PC9
481672400002	F/W ASSY;KBD CTRL,SCORPIO	U509
481672400001	F/W ASSY;SYS/VGA BIOS,SCORPIO	U10
340671200020	FAN ASSY;8170	
273000610019	FERRITE ARRAY;130OHM/100MHZ,3216	FA501
273000610019	FERRITE ARRAY;130OHM/100MHZ,3216	FA501
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L504,L512,L514,L516,L520,L
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L27,L504,L523,L554,PL5,PL5
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L1,L4,L513,L515
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L16,L17,L18,L19,L20,L21,L2
273000150036	FERRITE CHIP;32OHM/100MHZ,2012,S	L34,L35,L40,L545,L546,L547
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L28,L39,L43,L44,L45,L531,L
422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENU	

9. Spare Parts List - 16

Part Number	Description	Location(s)
341671200010	FINGER;EMI GROUND SMD FINGER,H=4	E501,E502
341671200010	FINGER;EMI GROUND SMD FINGER,H=4	E511,E518,E519,TP506
342671700001	FINGER;EMI GROUNDING SMD FINGER	E1,E10,E2,E4,E5,E7,E8,E9
342672400007	FINGER;EMI GROUNDING SMD FINGER	E501,E502,E503,E507,E520,
288003600001	FIR;HSDL3600#007,FRONT VIEW,10P,	U2
295000010105	FUSE;1A,NORMAL,1206,SMT	F1,F501,F503,F504
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF501
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF502
295000010029	FUSE;FAST,.75A,63V,1206,THIN FIL	PF501
345671700009	GASKET;BRACKET T/P,8575	
345671700010	GASKET;KB PLATE,8575	
345671700011	GASKET;KB PLATE-1,8575	
345671600016	GASKET;LCD-HINGE,8175	
345671700019	GASKET;MIC,8575	
345671700004	GASKET;USB,8575	
340671700006	HEATSINK ASSY;N/B,8575	
340671700016	HEATSINK ASSY;P4 CPU, 8575	
344600000824	IC CARD CON PART;68P,IC11SA-BD-P	
291000610032	IC SOCKET;32P,PLCC,TIN,W/O PEGS,	U10
331650047803	IC SOCKET;BGA-PGA478B-SKT	U1
282574373004	IC;74AHC373,OCT D-TRAN,TSSOP,20P	U8
282574186002	IC;74AHCT1G86,SINGLE,XOR,SOT23,S	U513
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP	U11
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,	U517
284501032001	IC;ADM1032,TEMPERATURE MTR,SO8	U2

Part Number	Description	Location(s)
284500201002	IC;ALC201,AC97 CODEC,TQFP,48P	U15
286308800006	IC;AME8800AEEV,VOL REG.,SOT23-5,	U17
286308801002	IC;AME8801MEEV,VOL REG.,SOT23-5,	U512
284508500002	IC;CM8500,3A BUS TERMINATOR,PTSS	PU10
283400000003	IC;EEPROM,NM24C02N,2K,SO,8P	U7
283450083001	IC;FLASH,256K*8-70,PLCC32,ST39SF	
284583437003	IC;H8/F3437S,KBD CTRL,TQFP,100P,	
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU507
284501893001	IC;ICS-1893,LAN-PHY,TQFP,64P,SMT	U5
284593722001	IC;ICS93722,DDR ZERO DELAY CLOCK	U9
284595200101	IC;ICS952001,TIMING CTL HUB FOR	U508
286300811002	IC;IMP811,RESET CIRCUIT,4.38,SOT	U515
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU514
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U506
286317099001	IC;LTC1709-9,PWM,QSOP,36P	PU508
286303707001	IC;LTC3707,PWM SWITCH REG,SOOP,2	PU4
286303707001	IC;LTC3707,PWM SWITCH REG,SOOP,2	PU510
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU1
286300809002	IC;MAX809S,RESET CIRCUIT,2.9V,SO	U12
286305258001	IC;MIC 5258-1.2BM5,LV12,LDO REG,	U502
284501284001	IC;PAC1284-01Q,TERMIN. NETWK,QSO	U501,U502
284587393002	IC;PC87393F,TQFP,100P	U511
284501410008	IC;PCI1410AGGU,BGA144P	U6
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U1,U3
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ510

9. Spare Parts List - 17

Part Number	Description	Location(s)
284500301004	IC;SIS301LV,TV ENCODER/LVDS,128P	U504
284500650002	IC;SIS650,N.B.,BGA702	U4
284500961003	IC;SIS961 HM-I/O,S.B.,BGA371	U14
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU511
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24	U16
286302211001	IC;TPS2211,POWER DISTRI SW,SSOP1	U505
284572872001	IC;UPD72872;IEEE1394;PQFP120,2PO	U18
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL2
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL4
273000990031	INDUCTOR;10UH,CDRH127B,SUMIDA,SM	PL3
273000990054	INDUCTOR;10UH,D124C,+/-20%,TOKO,	PL3
273000990115	INDUCTOR;3.3uH,3A,CSS054D,SMT	PL8
273000990021	INDUCTOR;33uH,CDRH124,SMT	PL6
273000150106	INDUCTOR;4.7UH,10%,2012,SMT	L2,L3
346671200036	INSULATOR,MDC,8170	
346671700001	INSULATOR;AL-FOIL,M/B BOTTOM,857	
346671700006	INSULATOR;CD-ROM,M-B,8575	
346669900004	INSULATOR;INVERTER,7170	
346671600018	INSULATOR;INVERTER,PCB,8175	
346671700007	INSULATOR;MINIPCI,8575	
346671600015	INSULATOR;PCMCIA,8175	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242662300009	LABEL;25*10MM,3020F	
242662300009	LABEL;25*10MM,3020F	

Part Number	Description	Location(s)
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D18,D19,D20,D21,D22,D23
421671600051	MICROPHONE ASSY;8175	
291006212402	MINIPCI SOCKET;124P,0.8MM,H=6,SM	J509
375102030010	NUT-HEX;M2,2,NIW	
375120262008	NUT-HEX;M2.6,NCG	
221671250005	PARTITION;HDD CASE,8170	
412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/	
316671200005	PCB;PWA-8170/ESB BD	R01
316671700002	PCB;PWA-8575/DD BD	R0B
316671700001	PCB;PWA-8575/M BD	R0B
316671700003	PCB;PWA-8575/TOUCHPAD BD	R00
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222667220003	PE BAG;L560XW345,CERES	
222670000001	PE BUBBLE BAG;BATTERY,7521	
273000150033	PHASEOUT;FERRITE CHIP,120OHM/100	L10,L11,L12,L13,L14,L15,L2
343671600006	PLATE;KB,8175	
411671200007	PWA;PWA-8170,ESB BD	
411671700007	PWA;PWA-8575,D/D BD R0A,SMT	
411671700006	PWA;PWA-8575,D/D BD R0A,T/U	
411671700010	PWA;PWA-8575,MOTHER R0A BD	
411671700013	PWA;PWA-8575,MOTHER R0B BD,SMT	
411671700014	PWA;PWA-8575,MOTHER R0B BD,T/U	
411671700009	PWA;PWA-8575,T/P BD	

9. Spare Parts List - 18

Part Number	Description	Location(s)
411503400201	PWA;PWA-STINGRAY/INVERTER BD,MSL	
271046037103	RES;.003,1.5W,1%,2512,SMT	PR501,PR503
271046057102	RES;.005,1.5W,1%,2512,SMT	PR502,PR504
271045087101	RES;.008 ,1W ,1% ,2512,SMT	PR16
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR4,PR506
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR525
271045157101	RES;.015 ,1W ,1% ,2512,SMT	PR515
271586026101	RES;.02 ,2W,1%,2512,SMT	PR13
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L2
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L513
271071000002	RES;0 ,1/16W,0603,SMT	PR17,PR522,PR523,R1,R511
271071000002	RES;0 ,1/16W,0603,SMT	C305,C723,L538,PR1,PR524,
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	R506,R579
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R64
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR3
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR514,PR521,R100,R101,R1(
271071101101	RES;100 ,1/16W,1% ,0603,SMT	R522,R536
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R231,R548,R566,R74,R789,R
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR557,PR563
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR508,PR518
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR15,PR3,PR510,PR538,PR5
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR12,PR19
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR507,PR513,PR527,PR540,
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R10,R516
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR506,R125,R138,R149,R15,

Part Number	Description	Location(s)
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R189
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R20
271071113101	RES;11K ,1/16W,1% ,0603,SMT	PR8
271071113101	RES;11K ,1/16W,1% ,0603,SMT	PR530
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	R578,R731,R732,R733,R734
271071127211	RES;12.7K,1/16W,1%,0603,SMT	PR508
271071137271	RES;13.7K,1/16W,.1%,0603,SMT	PR10,PR558
271071131101	RES;130 ,1/16W,1% ,0603,SMT	R545
271071134701	RES;130K ,1/16W,0.1% ,0603,SMT	PR560
271071147011	RES;147 ,1/16W,1% ,0603,SMT	R549
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R109,R116,R21,R508,R553,R
271071151302	RES;150 ,1/16W,5% ,0603,SMT	R503,R504
271071153101	RES;15K ,1/16W,1% ,0603,SMT	PR13,PR14
271071153101	RES;15K ,1/16W,1% ,0603,SMT	PR528,PR532,R720,R722
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R502,R503,R504,R505,R508,
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R107,R114,R269,R270
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR19,R556,R95
271071102302	RES;1K ,1/16W,5% ,0603,SMT	PR517
271071102302	RES;1K ,1/16W,5% ,0603,SMT	PR509,PR537,R1,R174,R194,
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR509,PR521,PR6,PR7,R528
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR5,PR505,PR539,PR545,PR
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R552,R558,R672,R674
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	PR546
271012278101	RES;2.7 ,1/8W,1% ,1206,SMT	R14
271071272101	RES;2.7K ,1/16W,1% ,0603,SMT	PR9

9. Spare Parts List - 19

Part Number	Description	Location(s)
271071272101	RES;2.7K ,1/16W,1% ,0603,SMT	PR531
271071272301	RES;2.7K ,1/16W,5% ,0603,SMT	R86,R87
271071200101	RES;20 ,1/16W,1% ,0603,SMT	R544
271072201101	RES;200 ,1/10W,1% ,0603,SMT	R57
271071204101	RES;200K ,1/16W,1% ,0603,SMT	PR18
271071203701	RES;20K ,1/16W,.1%,0603,SMT	PR7
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR12,PR519
271071203302	RES;20K ,1/16W,5% ,0603,SMT	R679,R719,R721
271071215211	RES;21.5K,1/16W,1% ,0603,SMT	PR526
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R117,R118,R119,R129,R130,
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR551
271071223302	RES;22K ,1/16W,5% ,0603,SMT	R49
271071249311	RES;249K ,1/16W,1% ,0603,SMT	PR547
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R509
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R577,R727,R728,R835
271071301011	RES;301 ,1/16W,1% ,0603,SMT	R12,R62
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR564
271071324211	RES;32.4K,1/16W,1% ,0603,SMT	PR5
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R9
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R16,R166,R167,R171,R172,R
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R2,R3,R506,R7
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR16,PR552,R697
271071390302	RES;39 ,1/16W,5% ,0603,SMT	R532
271072302301	RES;3K ,1/10W,5% ,0603,SMT	R739
271071475112	RES;4.75K,1/16W,1% ,0603,SMT	PR511

Part Number	Description	Location(s)
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR516
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR14,PR4,PR561,R120,R144,
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR11
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R137,R156,R157,R200,R201,
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR507,PR510
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R505,R683,R7
271071475011	RES;475 ,1/16W,1% ,0603,SMT	R85
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R4,R5,R518,R8
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR544,R134,R159
271071487311	RES;487K ,1/16W,1% ,0603,SMT	PR9
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R533,R535,R636,R640,R645,
271071518301	RES;5.1 ,1/16W,5% ,0603,SMT	PR17
271071512101	RES;5.1K ,1/16W,1% ,0603,SMT	R239
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R131,R140
271071510301	RES;51 ,1/16W,5% ,0603,SMT	PR2,R512,R513,R514,R515,R
271071511812	RES;51.1,1/16W,1% 0603,SMT	R14,R521
271071513301	RES;51K ,1/16W,5% ,0603,SMT	R184
271071536211	RES;53.6K,1/16W,1% ,0603,SMT	PR18
271071560101	RES;56 ,1/16W,1% ,0603,SMT	R41,R46,R605,R676
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R238,R240,R241,R243,R587,
271071576311	RES;576K ,1/16W,1% ,0603,SMT	PR556
271071604111	RES;6.04K,1/16W,1% ,0603,SMT	R550
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR543
271071681111	RES;6.81K,1/16W,1% ,0603,SMT	PR522
271071682301	RES;6.8K ,1/16W,5% ,0603,SMT	R185,R186,R187

9. Spare Parts List - 20

Part Number	Description	Location(s)
271071604811	RES;60.4 ,1/16W,1% ,0603,SMT	R50
271071619811	RES;61.9 ,1/16W,1% ,0603,SMT	R27,R30
271071620102	RES;62,1/16W,1% 0603,SMT	R10,R11,R528
271071681101	RES;680 ,1/16W,1% ,0603,SMT	R534
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R25,R562
271071750302	RES;75 ,1/16W,5% ,0603,SMT	R31,R35,R525,R537,R538,R5
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R190
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR518
271071820301	RES;82 ,1/16W,5% ,0603,SMT	R205,R207,R210,R777
271071909101	RES;9.09K,1/16W,1% ,0603,SMT	R228
271071976311	RES;976K ,1/16W,1% ,0603,SMT	PR8
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP1,RP2,RP3,RP4
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP48,RP501,RP503,RP504,R
271571000301	RP;0*8 ,16P ,1/16W,5% ,1606,SM	RP13,RP14,RP15
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	FA502,FA503,FA504,FA505,F
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP10,RP11,RP12,RP16,RP17
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP3,RP4,RP40,RP518,RP529
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP1
271621102302	RP;1K*8 ,10P,1/32W,5% ,1206,SMT	RP2,RP507
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP5,RP512,RP6
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP43,RP528
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SM	RP21,RP22,RP23,RP24,RP25
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP36,RP46,RP47,RP511,RP5
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP514,RP519
271621471301	RP;470*4,8P,1/16W,5%,1206,SMT	RP7

Part Number	Description	Location(s)
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP513,RP517
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP5
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP502
271621822302	RP;8.2K*8,10P,1/32W,5% ,1206,SMT	RP37,RP38,RP39
345671600002	RUBBER PAD;LCD,LOWER,8175	
345671600001	RUBBER PAD;LCD,UPPER,8175	
565167170001	S/W;CD ROM,SYSTEM DRIVER,8575	
340671200013	SCREW ASSY;CPU,8170	
340671200014	SCREW ASSY;IC,82845,8170	
371102011502	SCREW;M2L15,FLT(+),NIW/NLK	
340671700007	SHIELDING ASSY;TOP,8575	
341671700001	SHIELDING;AUDIO,8575	
370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102010309	SPC-SCREW;M2L3.0,NIW/NLK,HD07	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010606	SPC-SCREW;M2L6,K-HD(t0.2),NIB/NL	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYL	

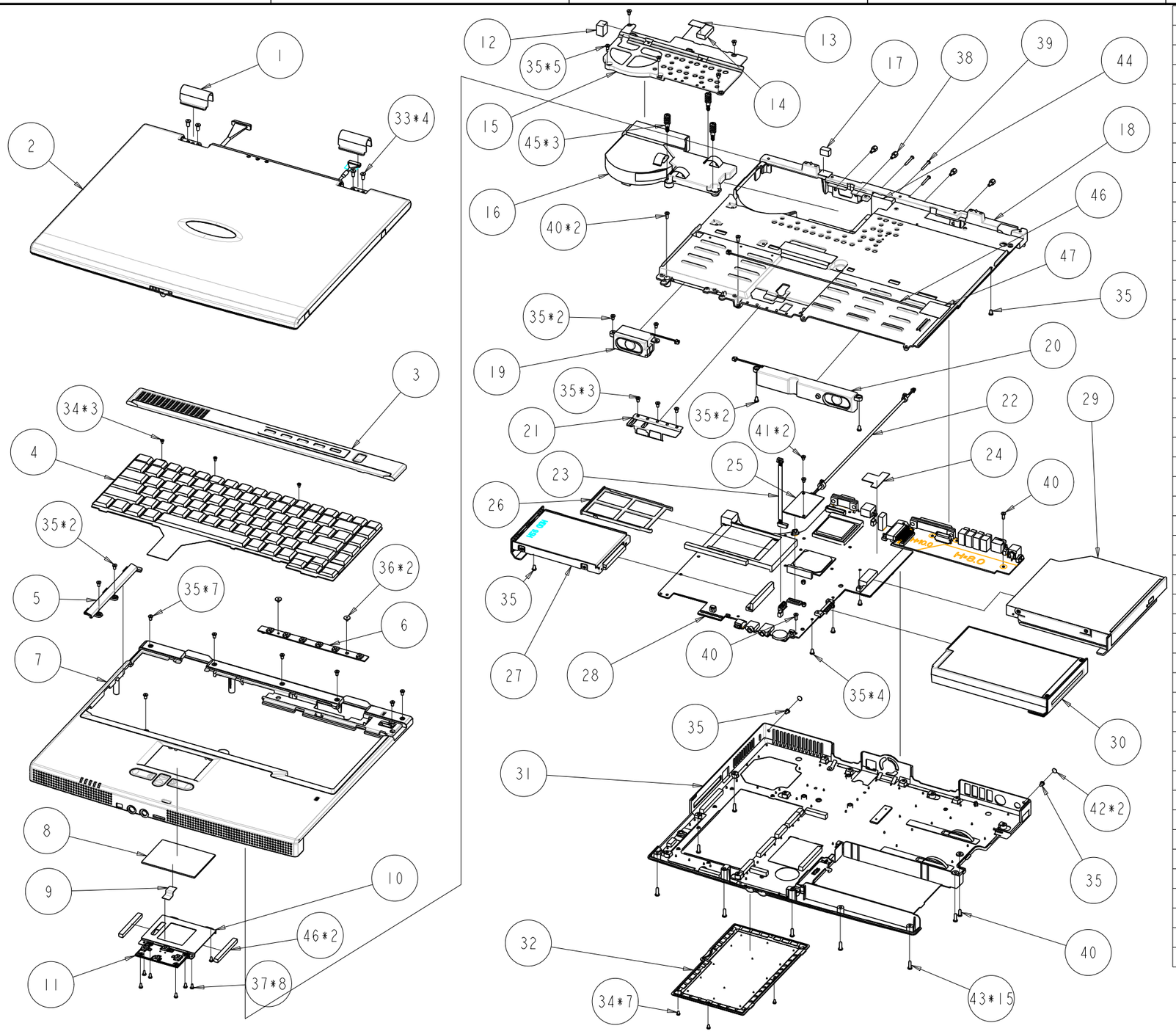
9. Spare Parts List - 21

Part Number	Description	Location(s)
340671700003	SPEAKER ASSY,L,8575	
340671700008	SPEAKER ASSY;R,8575	
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	
341668300008	STANDOFF;MDC MODEM,NLK,HOPE	
297120101007	SW;DIP,SPST,4P,24VDC,.025A,SMT	SW503
297040105012	SW;PUSH BUTTOM,4P,SP,12V/50MA,H2	SW502
297040105012	SW;PUSH BUTTOM,4P,SP,12V/50MA,H2	SW1,SW2,SW3,SW4,SW5,SW6
297040105010	SW;PUSH BUTTOM,5P,SPST,12V/50MA,	SW1,SW2,SW3,SW4
297030102001	SW;TOGGLE,SPST,5V/0.2mA,H10.7MM,	SW1
225600000004	TAPE;DOUBLE SIDE,12MM*15M	
345671700002	THERMAL PAD;MOS,8575	
345671700003	THERMAL PAD;SIS301,8575	
442164900010	TOUCH PAD MODULE;TM41PD-350	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ2,PQ501,PQ502,PQ503
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ4,PQ501,PQ502,PQ504,PQ
288203401001	TRANS;AO3401,P-MOSFET,SOT-23	PQ1
288203401001	TRANS;AO3401,P-MOSFET,SOT-23	Q1,Q509,Q511,Q6,Q8
288200144002	TRANS;DTA144WK,PNP,SMT	PQ506,Q529
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q10,Q11,Q17,Q18,Q19,Q2,Q
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ509,Q20,Q5,Q510,Q9
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ3
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q15,Q516,Q517
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q14
288207002001	TRANS;NDC7002N,N-MOSFET,SSOT-6	PQ2
288202302001	TRANS;SI2302DS,N-MOSFET,SOT-23	Q534

Part Number	Description	Location(s)
288204416001	TRANS;Si4416DY,N-MOSFET,.028OHM,	PU2,PU5
288204416001	TRANS;Si4416DY,N-MOSFET,.028OHM,	PU507,PU509
288204425002	TRANS;SI4425DY,PMOS,8.5A/30V,.02	PU502
288204425002	TRANS;SI4425DY,PMOS,8.5A/30V,.02	PU512,PU513
288204788001	TRANS;SI4788CY,P-MOS,5A1.8~5.5V,	PU504,PU505
288204810001	TRANS;SI4810DY,N-MOS,.0155OHM,SO	PU3,PU6
288204810001	TRANS;SI4810DY,N-MOS,.0155OHM,SO	PU7,PU8
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PQ1
288204925001	TRANS;SI4925DY,P-MOSFET,SO-8	PU9
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,S	Q503
288205003004	TRANS;SUD50N03-11,N-MOS,TO252	PU1,PU2,PU4,PU5,PU501,PU
273001050039	TRANSFORMER;10/100 BASE,LF-H80P,	U3
271911103906	VR;10K,20%,0.05W,RN101GAC10KPGJ-	VR1
421671700002	WIRE ASSY;ANTENNA,8575	
421668300005	WIRE ASSY;BIOS,BATTERY,HOPE	J508
421668300005	WIRE ASSY;BIOS,BATTERY,HOPE	J508
421671600010	WIRE ASSY;INVERT,8175	
421671700004	WIRE ASSY;MDC,EMI,8575	
421671700001	WIRE ASSY;TOUCHPAD,8575	
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,S	X502
274011431422	XTAL;14.318MHZ,16PF,20PPM,8*4.25	X501
274011600408	XTAL;16MHZ,16PF,50PPM,8*4.5,2P	X503
274012457405	XTAL;24.576M,30PPM,16PF,7*5,4P,S	X6
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X3
274012500401	XTAL;25MHZ,30PPM,18PF,4P,SMT	X1,X4

9. Spare Parts List - 22

Part Number	Description	Location(s)
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM20	X5



ITEM	PART NO.	DESCRIPTION	Q'TY	REMARK
1	344671600011	COVER;HINGE,8175	2	
2	441671730005	LCD ASSY;QD1,XGA,14.1",ID4,8575	1	OPTION
3	340671700015	KEYBOARD COVER;ASSY-B,8575	1	
4	5310999990128	KBD OPTION;86,US,8175	1	OPTION
5	344671600010	COVER;DUMMY,8175	1	
6	411671200007	PCB;QUICK KEY,8170	1	
7	340671700001	COVER ASSY;8575	1	
8	442164900010	TOUCH PAD MODULE;TM41PD-350	1	
9	422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENUS	1	
10	340671600028	BRACKET ASSY;T/P,INSULATOR,8175	1	
11	411671200006	PWA;PWA-8170,T/P BD	1	
12	345671600018	GASKET;HEATSINK,K/B_PLATE,8175	1	
13	345671700010	GASKET;KB PLATE,8575	1	
14	345671700011	GASKET;KB PLATE-1,8575	1	
15	343671600006	PLATE;KB,8175	1	
16	340671700016	HEATSINK ASSY;P4 CPU,8575	1	
17	345671600016	GASKET;LCD-HINGE,8175	1	
18	340671700007	SHIELDING ASSY;TOP,8575	1	
19	340671700003	SPEAKER ASSY;L,8575	1	
20	340671700008	SPEAKER ASSY;R,8575	1	
21	341671700001	SHIELDING;AUDIO,8575	1	
22	421671700004	WIRE ASSY;MDC,EMI,8575	1	
23	421671700001	WIRE ASSY;TOUCHPAD,8575	1	
24	345671700002	THERMAL PAD;MOS,8575	1	
25	412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/KIT	1	
26	344671600043	DUMMY CARD;PCMCIA,8175	1	
27	523467170009	HDD ASSY;30G,2.5",9.5MM,8575	1	OPTION
28	411671700010	PWA;PWA-8575,MOTHER BD	1	
29	523467160014	DVD ROM ASSY;8X,SDR-081,QUANTA,8175	1	OPTION
30	441999900062	BATT ASSY OPTION;LI,9-CELL,8575	1	OPTION
31	340671700002	HOUSING ASSY;8575	1	
32	340671600012	COVER ASSY;DIMM,8175	1	
33	370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYLOK	4	
34	370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	10	
35	370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	29	
36	370102010309	SPC-SCREW;M2L3.0,NIW/NLK,HD07	2	
37	370102010407	SPC-SCREW;M2L4,K-HD,t=1.1,NIB	8	
38	377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	4	
39	371102011502	SCREW;M2L15,FLT(+),NIW/NLK	3	
40	370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	5	
41	370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	2	
42	346671700021	INSULATOR;REAR,SCREW,8575	2	
43	370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,t=1.1,NIB	15	
44	340671200020	FAN ASSY;8170	1	
45	340671200013	SCREW ASSY;CPU,8170	3	
46	421671600051	MICROPHONE ASSY;8175	1	
47	345671700019	GASKET;MIC,8575	1	
48	345671700009	GASKET;BRACKET T/P,8575	2	

ITEM	CONTENTS OF CHANGE	CHK	APV	MM/DD/YY

TOL ± / RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

SCALE 0.200

DATE	16-Jun-02	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.053	DRAWING NAME	LT PF;QD1,XGA,14.1",ID4,8575	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	416267173006 R00

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SHEET NO.1 OF 1

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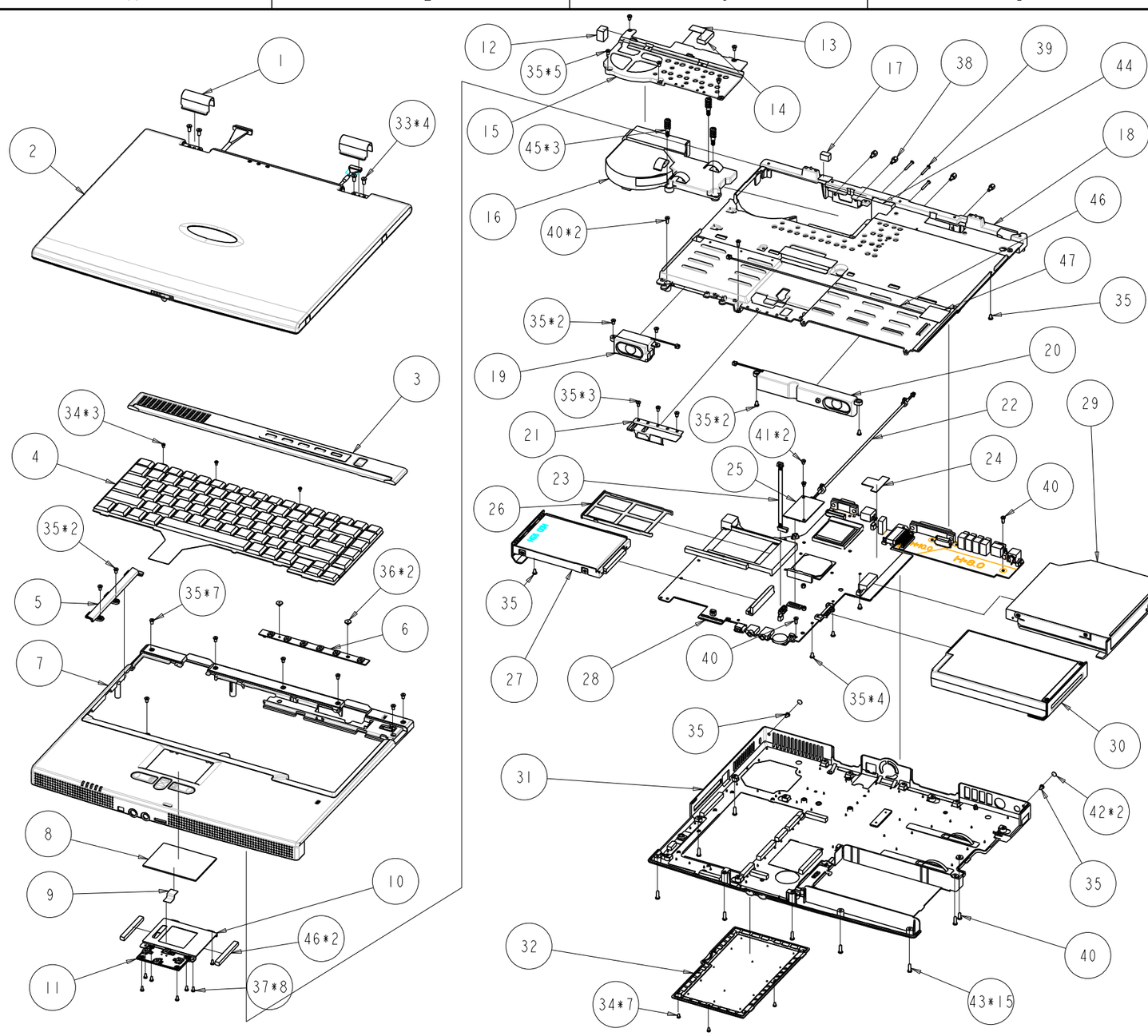

ITEM	PART NO.	DESCRIPTION	Q'TY	REMARK
1	344671600046	COVER;HINGE,IDI-2,8175	2	
2	441671740005	LCD ASSY;QDI,XGA,14.1",ID5,8575	1	OPTION
3	340671700014	KEYBOARD COVER;ASSY-S,8575	1	
4	531099990128	KBD OPTION;86,US,8175	1	OPTION
5	344671600042	COVER;DUMMY,IDI-2,8175	1	
6	411671200007	PCB;PWA-8170,ESB BD	1	
7	340671710001	COVER ASSY;SILVER,8575	1	
8	442164900010	TOUCH PAD MODULE;TM41PD-350	1	
9	422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENUS	1	
10	340671600028	BRACKET ASSY;T/P,INSULATOR,8175	1	
11	411671700009	PWA;PWA-8575,T/P BD	1	
12	345671600018	GASKET;HEATSINK,K/B_PLATE,8175	1	
13	345671700010	GASKET;KB PLATE,8575	1	
14	345671700011	GASKET;KB PLATE-1,8575	1	
15	343671600006	PLATE;KB,8175	1	
16	340671700016	HEATSINK ASSY;P4 CPU,8575	1	
17	345671600016	GASKET;LCD-HINGE,8175	1	
18	340671700007	SHIELDING ASSY;TOP,8575	1	
19	340671700003	SPEAKER ASSY;L,8575	1	
20	340671700008	SPEAKER ASSY;R,8575	1	
21	341671700001	SHIELDING;AUDIO,8575	1	
22	421671700004	WIRE ASSY;MDC,EMI,8575	1	
23	421671700001	WIRE ASSY;TOUCHPAD,8575	1	
24	345671700002	THERMAL PAD;MOS,8575	1	
25	412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/KIT	1	
26	344671600043	DUMMY CARD;PCMCIA,8175	1	
27	523467170009	HDD ASSY;30G,2.5",9.5MM,8575	1	OPTION
28	411671700010	PWA;PWA-8575,MOTHER BD	1	
29	523467160014	DVD ROM ASSY;8X,SDR-081,QUANTA,8175	1	OPTION
30	441999900062	BATT ASSY OPTION;LI,9-CELL,8575	1	OPTION
31	340671700002	HOUSING ASSY;8575	1	
32	340671600012	COVER ASSY;DIMM,8175	1	
33	370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYLOK	4	
34	370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	10	
35	370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	29	
36	370102010309	SPC-SCREW;M2L3.0,NIW/NLK,HD07	2	
37	370102010407	SPC-SCREW;M2L4,K-HD,t=1.1,NIB	8	
38	377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	4	
39	371102011502	SCREW;M2L15,FLT(+),NIW/NLK	3	
40	370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	5	
41	370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	2	
42	346671700021	INSULATOR;REAR,SCREW,8575	2	
43	370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,t=1.1,NIB	15	
44	340671200020	FAN ASSY;8170	1	
45	340671200013	SCREW ASSY;CPU,8170	3	
46	421671600051	MICROPHONE ASSY;8175	1	
47	345671700019	GASKET;MIC,8575	1	
48	345671700009	GASKET;BRACKET T/P,8575	2	

ITEM	CONTENTS OF CHANGE	CHK	APV	MM/DD/YY

TOL ± RANGE	MI	M2	SI	S2	PI	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

SCALE 0.200

DATE	17-Jun-02	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.053	DRAWING NAME	LT PF;QDI,XGA,14.1",ID5,8575		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	416267174006	R00

MiTAC International Corp.

Model name:MAIN-ASSY-8575

File name:MAIN-ASSY-ID5-8575

SHEET NO.1 OF 1

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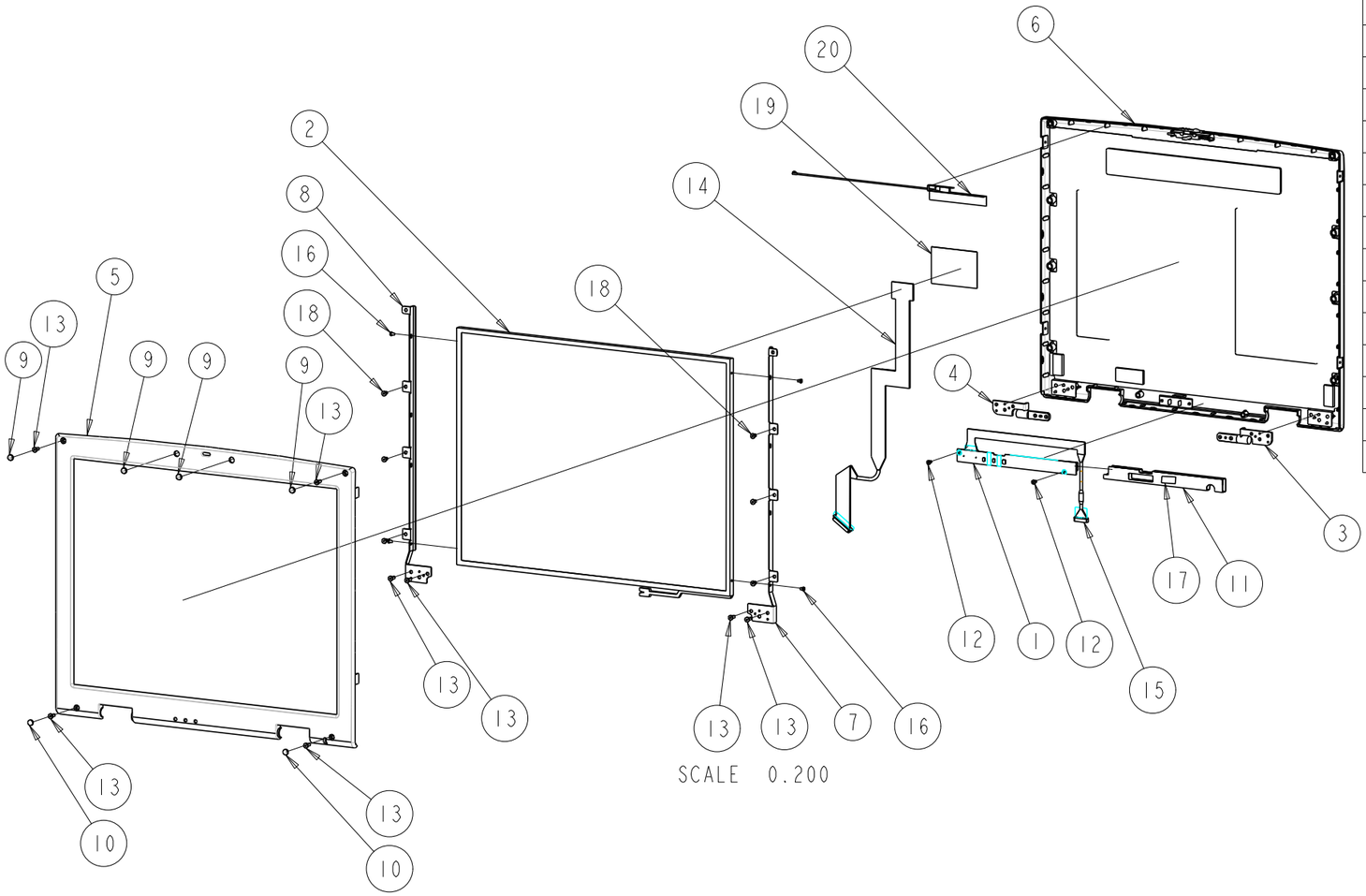

ITEM	PART NO.	DESCRIPTION	Q'TY	REMARK
1	411503400201	PWA;PWA-STINGRAY/INVERTER BD,MSL	1	
2	413000020304	LCD;QD114IX1LH03,TFT,14.1",LCDS,XGA,QUANTA-MP03	1	
3	340671600018	HINGE;R,14",8175	1	
4	340671600020	HINGE;L,14",8175	1	
5	340671720010	COVER ASSY;LCD,14",ID3,8575	1	
6	340671720003	HOUSING ASSY;LCD,14",ID3,8575	1	
7	342671600005	BRACKET;LCD,R,14",8175	1	
8	342671600007	BRACKET;LCD,14",8175	1	
9	345671600001	RUBBER PAD;LCD,UPPER,8175	4	
10	345671600002	RUBBER PAD;LCD,LOWER,8175	2	
11	346669900004	INSULATOR;INVERTER,7170	1	
12	370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	2	
13	370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	8	
14	421671600006	WIRE ASSY;LCD,UNIPAC,14",XGA,8175	1	
15	421671600010	WIRE ASSY;INVERT,8175	1	
16	370102030301	SPC-SCREW;M2L3,K-HD,1,NIB.NLK	4	
17	242664800013	LABEL;CAUTION,INVERT BD,PITCHING	1	
18	370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	6	
19	343671600014	AL-FOIL;HST-PANEL_15"-XGA,8175	1	
20	421671700002	WIRE ASSY;ANTENNA,8575	1	

ITEM	CONTENTS OF CHANGE	CHK	APV	MM/DD/YY

TOL ± / RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

DATE	19-Jun-02	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.050	DRAWING NAME	LCD ASSY;QD1,XGA,14.1",ID3,8575	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	441671720033 R00

MiTAC International Corp.

SHEET NO.1 OF 1

Model name:8575-ASSY-LCD

File name:8575-ASSY-LCD

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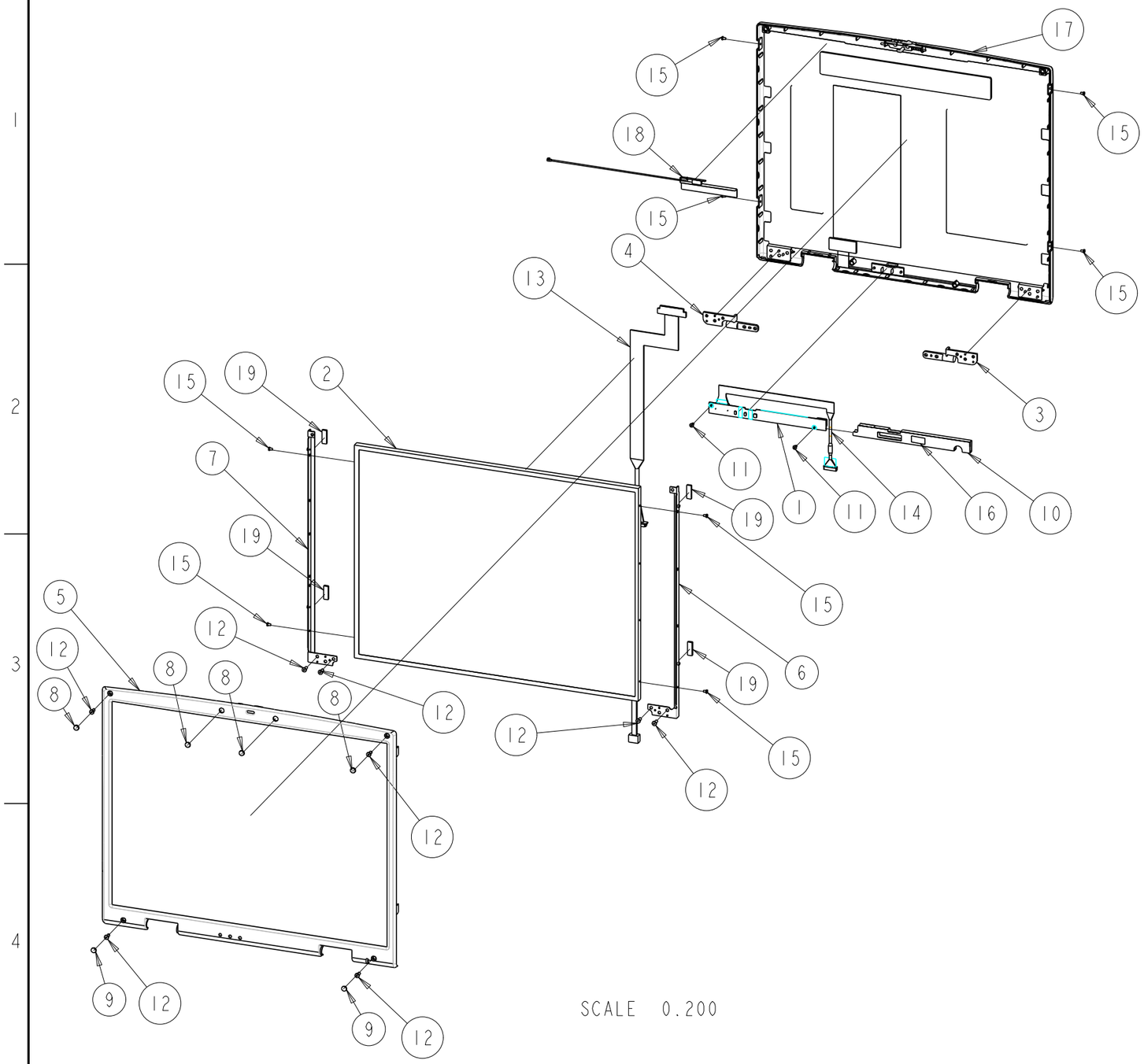

ITEM	PART NO.	DESCRIPTION	Q'TY	REMARK
1	411503400201	PWA;PWA-STINGRAY/INVERTER BD,MSL	1	
2	413000020317	LCD;HSD 150PX11-B,TFT,15",LVDS,XGA,HANNSTAR	1	
3	340671600017	HINGE;R,15",8175	1	
4	340671600019	HINGE;L,15",8175	1	
5	340671720009	COVER ASSY;LCD,15",ID3,8575	1	
6	342671600004	BRACKET;LCD,R,15",8175	1	
7	342671600006	BRACKET;LCD,L,15",8175	1	
8	345671600001	RUBBER PAD;LCD,UPPER,8175	4	
9	345671600002	RUBBER PAD;LCD,LOWER,8175	2	
10	346669900004	INSULATOR;INVERTER,7170	1	
11	370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	2	
12	370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	8	
13	421671600004	WIRE ASSY;LCD,HANN,15",XGA,8175	1	
14	421671600010	WIRE ASSY;INVERT,8175	1	
15	370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	8	
16	242664800013	LABEL;CAUTION,INVERT BD,PITCHING	1	
17	340671720002	HOUSING ASSY;LCD,15",ID3,8575	1	
18	421671700002	WIRE ASSY;ANTENNA,8575	1	
19	345671700006	GASKET;BRACKET LCD,8575	4	

ITEM	CONTENTS OF CHANGE	CHK	APV	MM/DD/YY

TOL ± / RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

DATE	19-Jun-02	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.048	DRAWING NAME	LCD ASSY;HANNSTAR,XGA,15.1",ID3,8575	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	441671720035 R00

MiTAC International Corp.

Model name:8575-ASSY-LCD

File name:LCD-ASSY-HANNSTAR-15-ID3-8575

SHEET NO.1 OF 1

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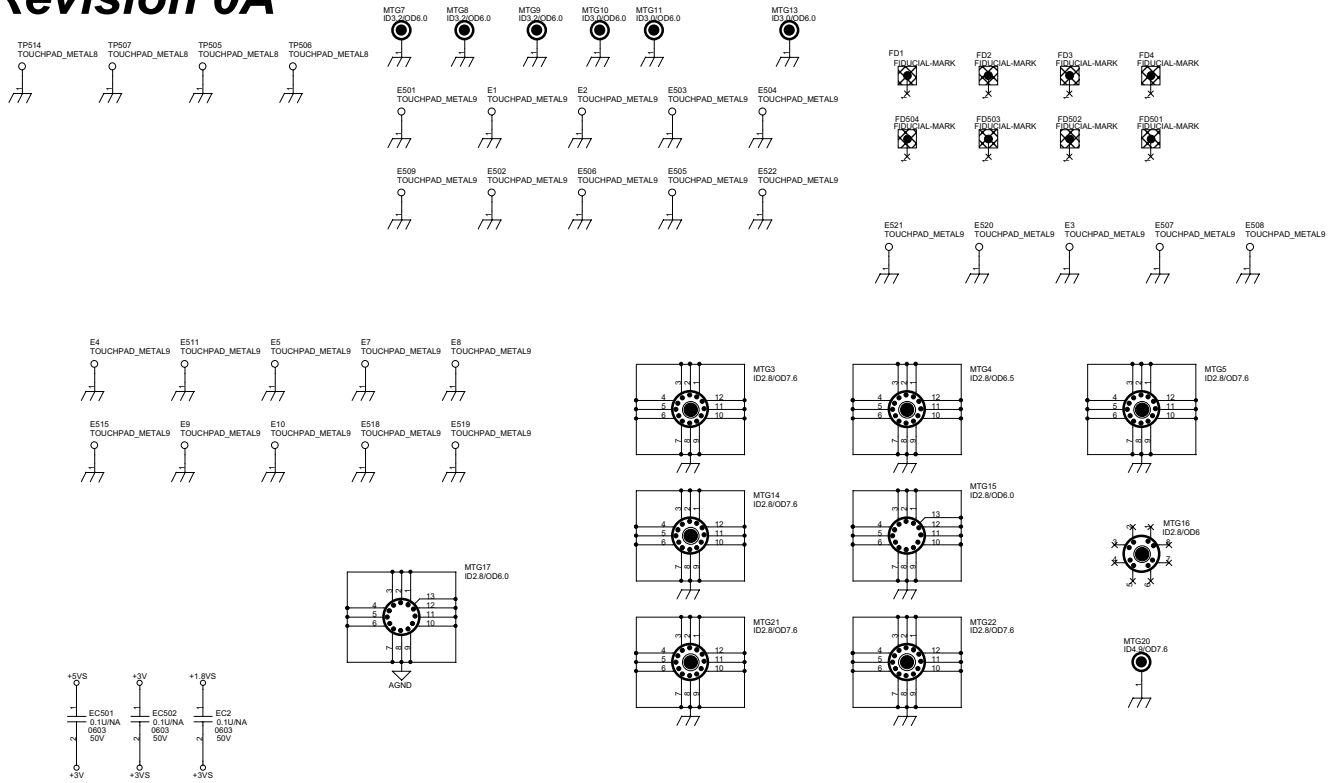
MODEL : 8575 AND 8575N Revision 0A

Contexts

Title	Page
COVER SHEET & SCREW HOLE	1
System Block Diagram	2
Power Block Diagram	3
P4-CPU (1/2)	4
P4-CPU (2/2)	5
SIS650(1/3)	6
SIS650(2/3)	7
SIS650(3/3)	8
TV/LVDS ENCODER(SiS301LV)	9
LCD/VGA INTERFACE & LEDs	10
MAIN CLOCK & CLOCK BUFFER	11
DDR SODIMMs	12
DDR TERMINATION	13
SIS961(1/3)	14
SIS961(2/3)	15
SIS961(3/3)	16
IDE INETRFACE & PULL-UPs	17
PCI1410 & CARDBUS SOCKET	18
LAN PHY (ICS 1893) & MDC	19
AUDIO CODEC & AUDIO AMP	20
SUPER I/O, T/P & BUTTON	21
MICROCONTROLLER (H8)	22
1.25 POWER (CM8500) & BAT CON	23
1.8V/2.5V POWER (LTC3707)	24
CHARGER (TL594C)	25
CPU POWER (LTC1709EG-7)	26
D/D CONNECTOR & MISC	27
MINI-PCI & BLUETOOTH	28
IEEE1394 (uPD72872)	29

DRAW	DESIGN	CHECK	ISSUED



POWER STATES

STATE / SIGNAL	VOTAGE	FULL ON	STR	STD	MEC-OFF	REMARK
-SUSB	-	HIGH	LOW	LOW	LOW	
-SUSC	-	HIGH	HIGH	LOW	LOW	
ADP	+19V	O	O	O	O	
BATTERY	+12V	O	O	O	O	
+VCC_RTC	+3.3V	O	O	O	O	
+VCC_CORE	+1.75V	O	O	X	X	
+1.8VS	+1.8V	O	X	X	X	
+1.8V	+1.8V	O	O	X	X	
+2.5V_DDR	+2.5V	O	O	X	X	
+3VS	+3.3V	O	X	X	X	
+3V	+3.3V	O	O	X	X	
+3VA	+3.3V	O	O	O	0	
+5VS	+5V	O	X	X	X	
+5V	+5V	O	O	X	X	
+5VA	+5V	O	O	0	0	
+12VS	+12V	O	X	X	X	
+12V	+12V	O	O	X	X	

IDSEL

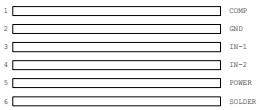
IDSEL	CHIP
AD20	PCI1410
AD21	MINIPCI
AD22	1394(uPD72872)

BUS MASTER

REQ/GNT	CHIP
-REQ0/-GNT0	PCI1410
-REQ1/-GNT1	1394(uPD72872)
-REQ2/-GNT2	MINIPCI

PCIINT

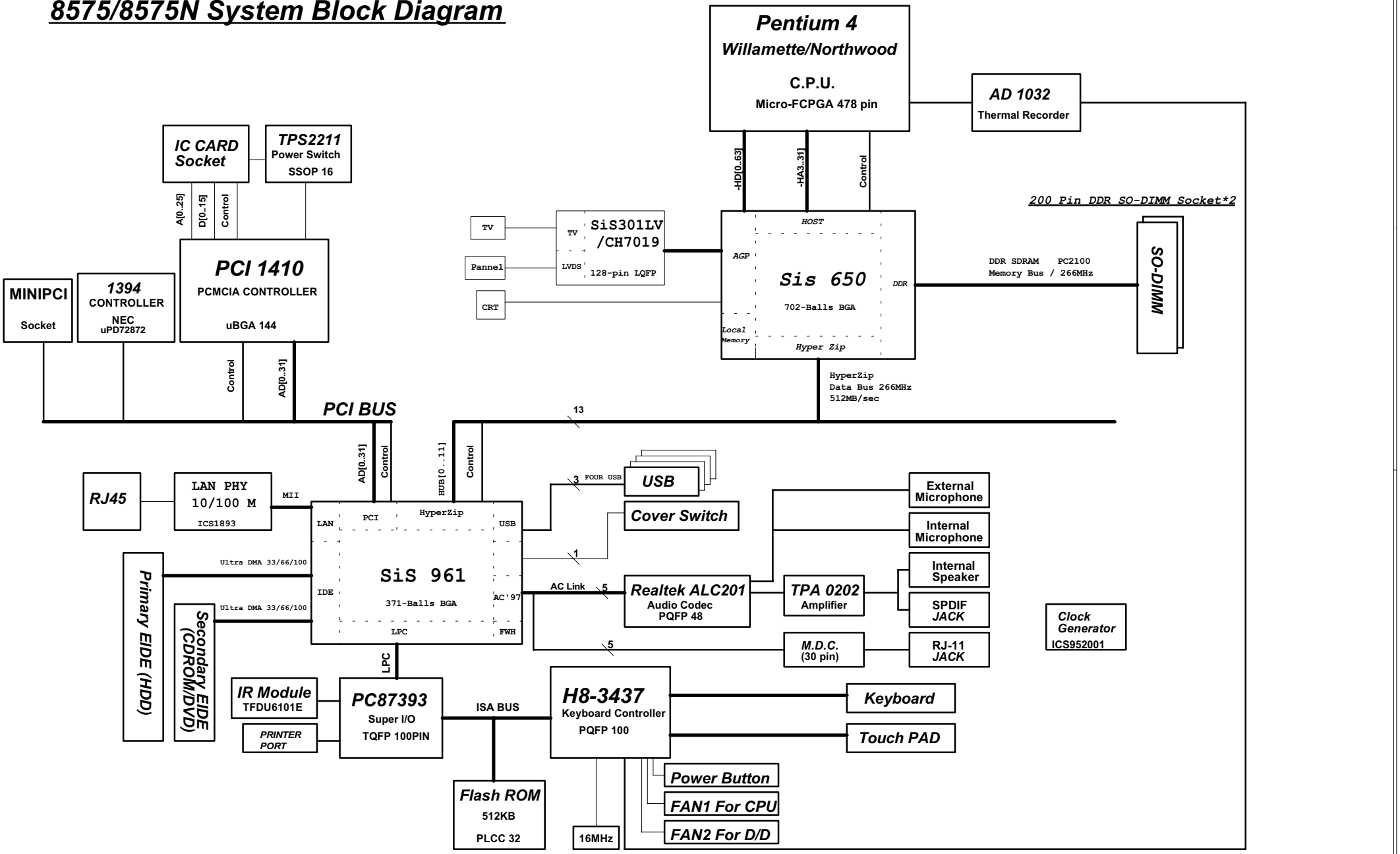
PCIINT	CHIP
INTA#	SiS650
INTB#	PCI1410
INTC#	1394(uPD72872)
INTD#	MINIPCI



MiTAC

Title	8575 COVER SHEET & SCREW HOLE	
Size C	Document Number 411671700010	Rev 0A
Date: Wednesday, January 16, 2002	Sheet 1 of 29	

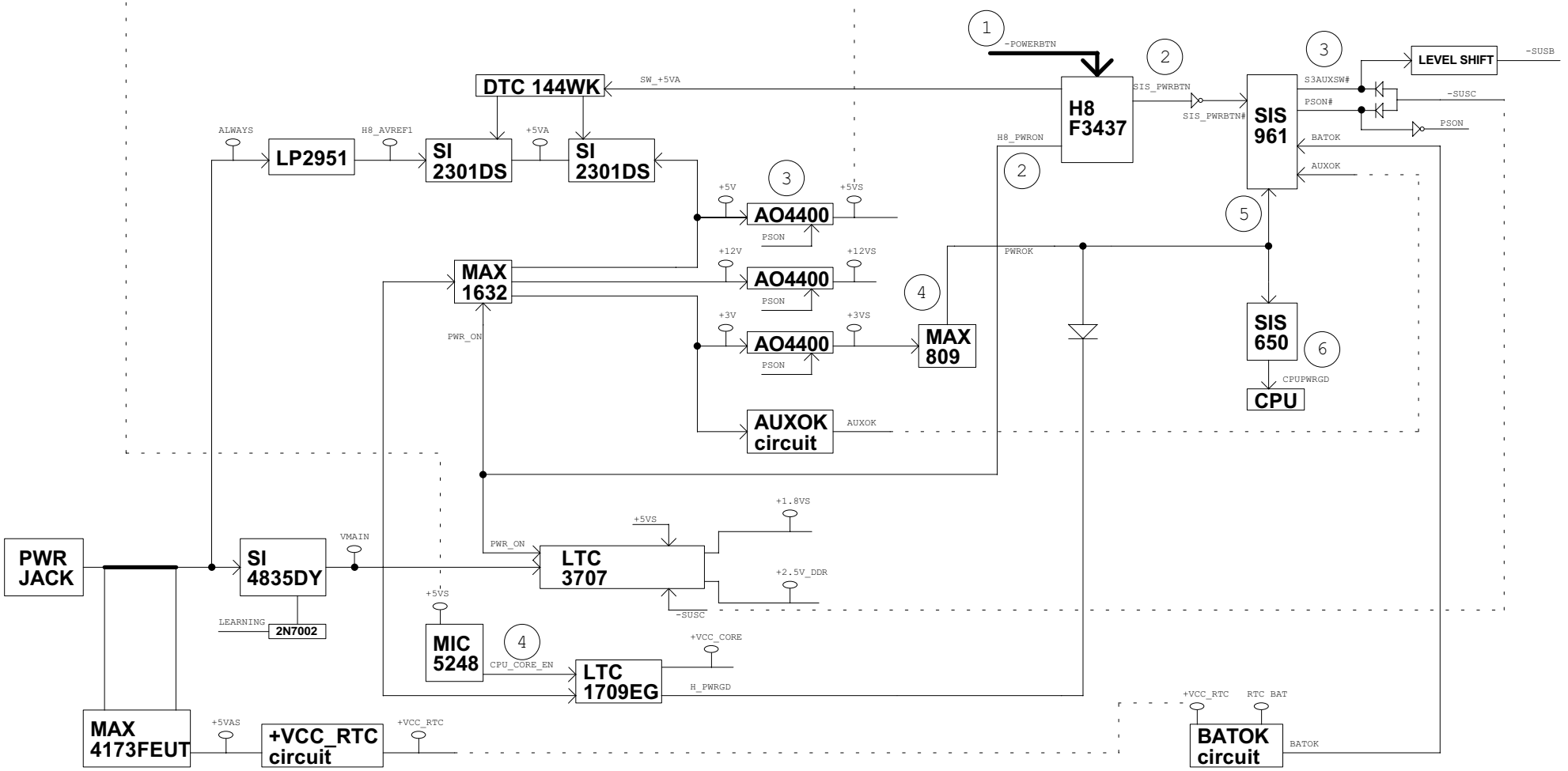
8575/8575N System Block Diagram



MiTAC

Title	8575 SYSTEM BLOCK DIAGRAM	
Size	Document Number 411671700010	Rev 0A
Date: Wednesday, January 16, 2002	Sheet 2 of 29	

POWER DIAGRAM OF THE PROJECT 8575



電子訊號線

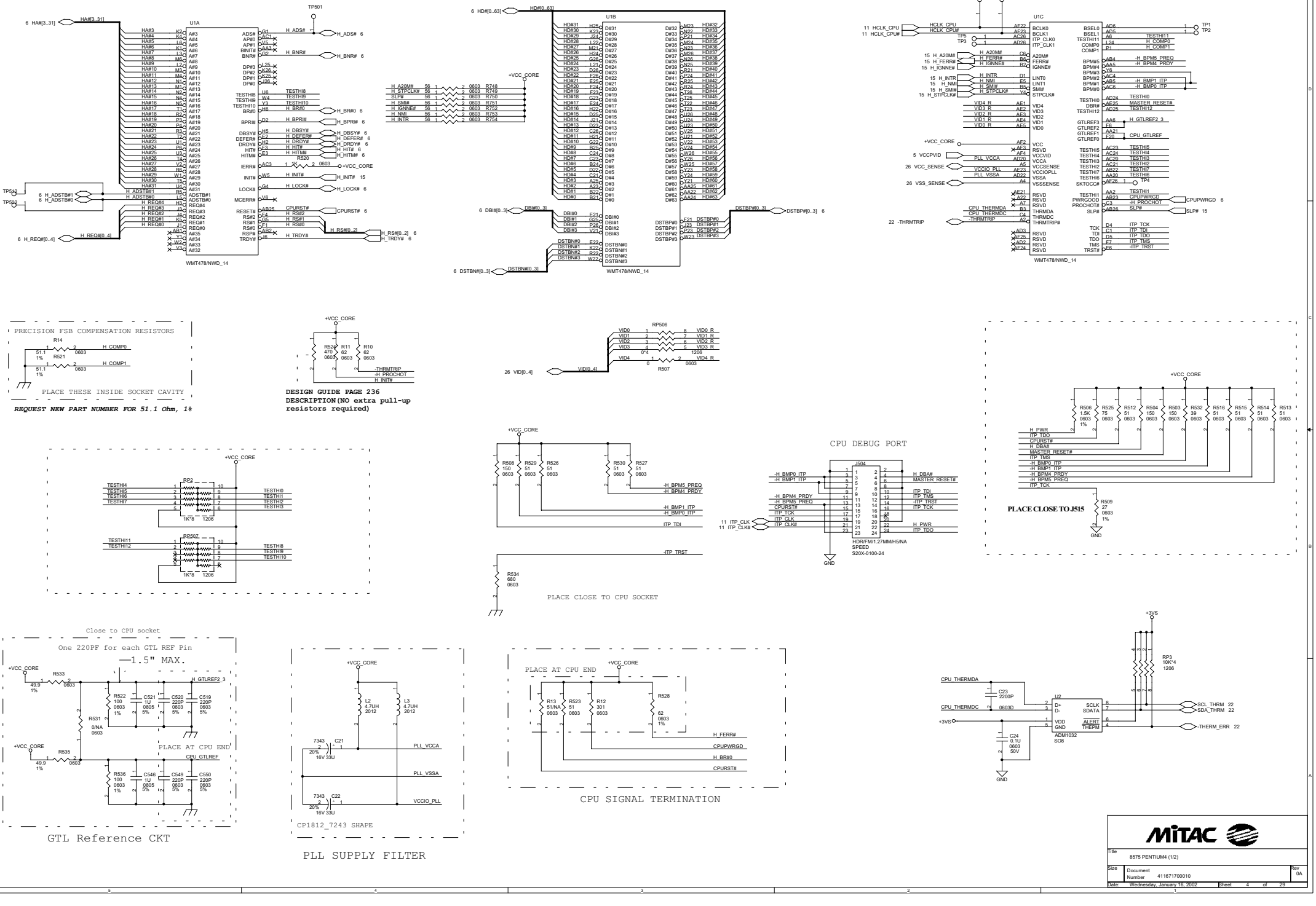
視線輔助線

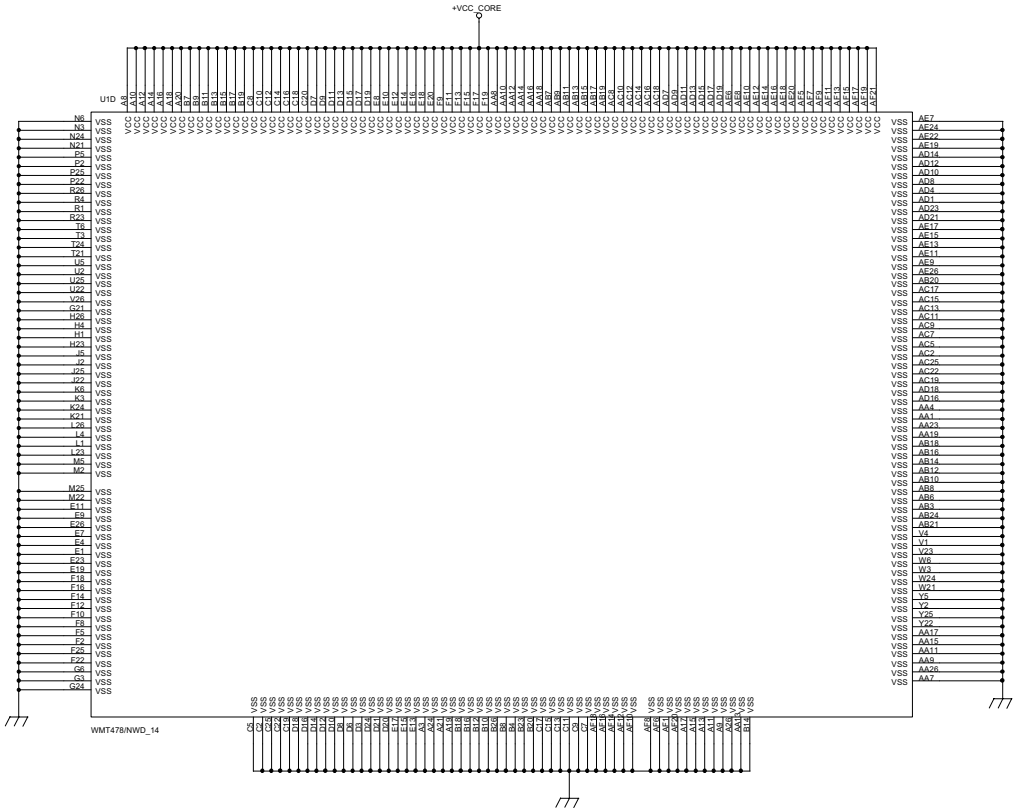
MiTAC

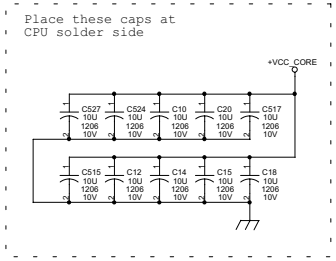
Title: 8575 POWER BLOCK DIAGRAM

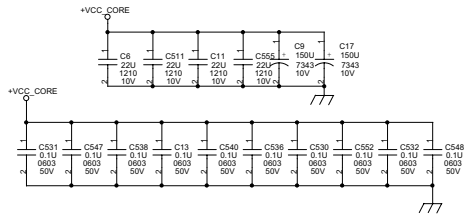
Size | Document Number 411671700010 | Rev 0A

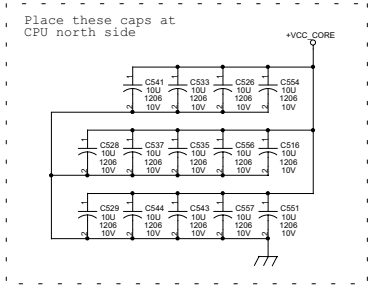
Date: Wednesday, January 16, 2002 | Sheet 3 of 29

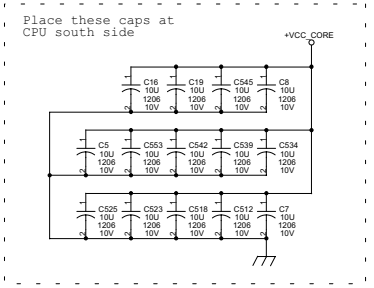

U1A
WMT478/NWD_14
U1B
WMT478/NWD_14
U1C
WMT478/NWD_14
TP501
TP503
TP504
PRECISION FSB COMPENSATION RESISTORS
PLACE THESE INSIDE SOCKET CAVITY
REQUEST NEW PART NUMBER FOR 51.1 Ohm, 1%
DESIGN GUIDE PAGE 236
DESCRIPTION(NO extra pull-up
resistors required)
RP506
RP2
RP507
PLACE CLOSE TO CPU SOCKET
CPU DEBUG PORT
J504
HDR/FM/1.27MM/H5/NA
SPEED
S20X-0100-24
PLACE CLOSE TO J515
Close to CPU socket
One 220PF for each GTL REF Pin
—1.5" MAX.
PLACE AT CPU END
GTL Reference CKT
CP1812_7243 SHAPE
PLL SUPPLY FILTER
PLACE AT CPU END
CPU SIGNAL TERMINATION
ADM1032
SO8
RP3
10K*4
1206
MiTAC
Title
8575 PENTIUM4 (1/2)
Size
Document
Number
411671700010
Rev
0A
Date:
Wednesday, January 16, 2002
Sheet
4
of
29

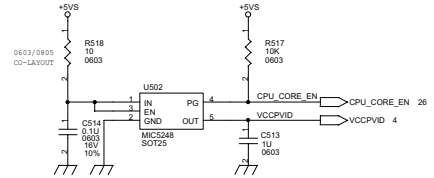








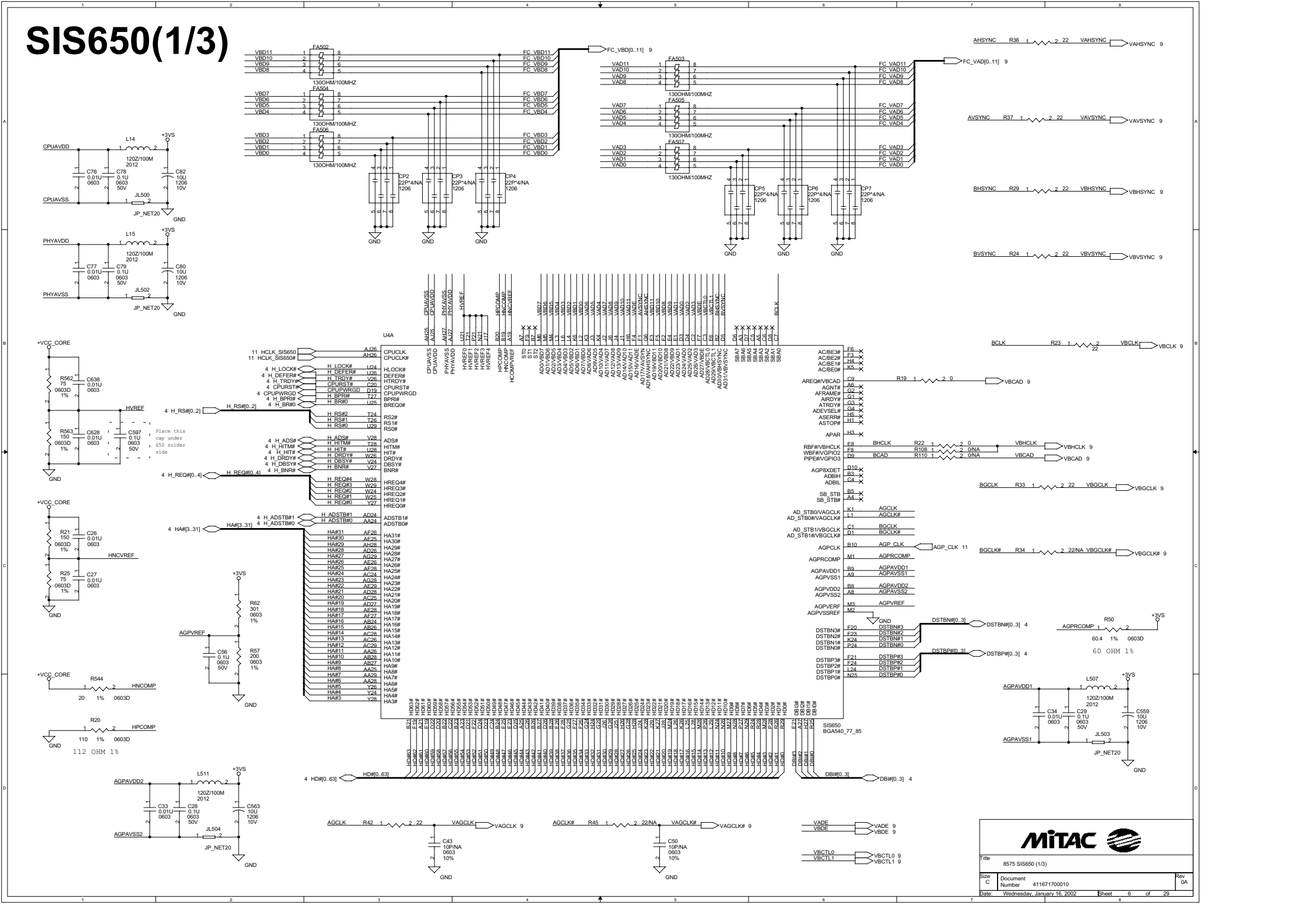




MiTAC

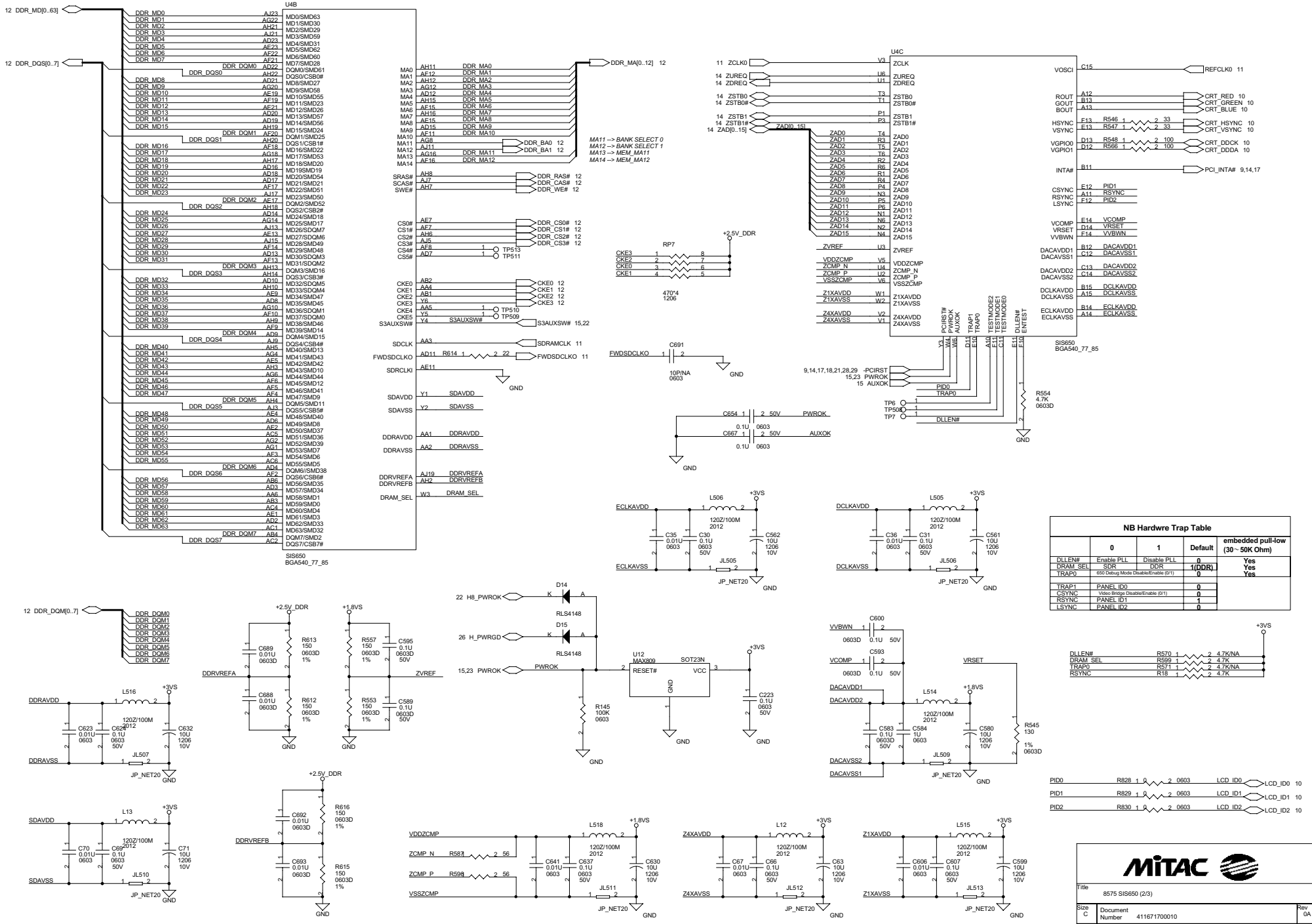
Title	8575 PENTIUM4 (2/2)
Size	Document Number 411671700010
Rev	0A
Date:	Wednesday, January 16, 2002
Sheet	5 of 29

SIS650(1/3)

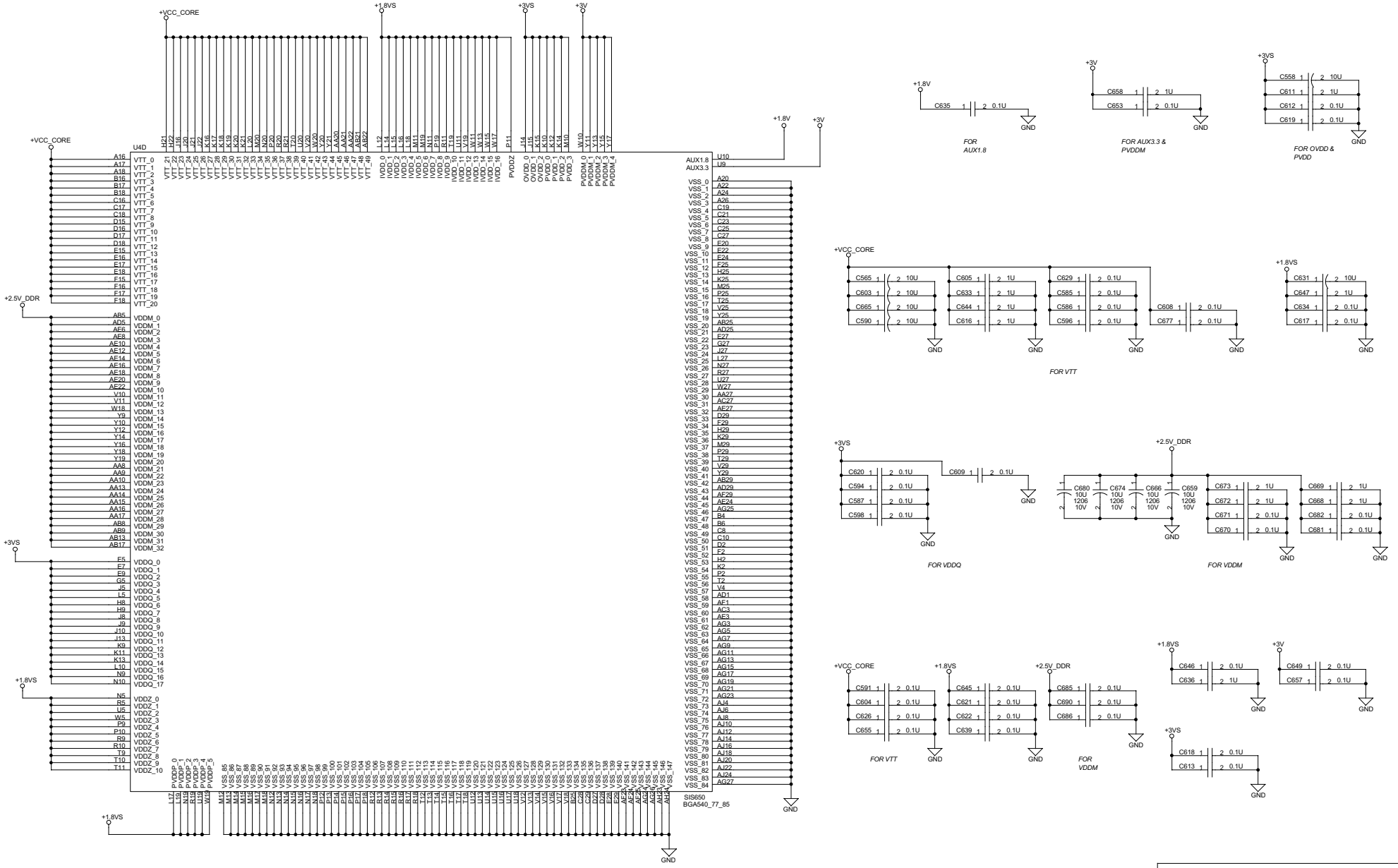


Title	8575 SIS650 (1/3)
Size	C
Document Number	411671700010
Rev	0A
Date:	Wednesday, January 16, 2002
Sheet	6 of 29

SIS650(2/3)


U4B
SIS650
BGA540_77_85
U4C
SIS650
BGA540_77_85
NB Hardwre Trap Table
DLLEN# Enable PLL Disable PLL 0 Yes
DRAM_SEL SDR DDR 1(DDR) Yes
TRAP0 650 Debug Mode Disable/Enable (0/1) 0 Yes
TRAP1 PANEL ID0 0
CSYNC Video Bridge Disable/Enable (0/1) 0
RSYNC PANEL ID1 1
LSYNC PANEL ID2 0
8575 SIS650 (2/3)
Size C
Document Number 411671700010
Rev 0A
Date: Wednesday, January 16, 2002
Sheet 7 of 29

SIS650(3/3)



Title	8575 SIS650 (3/3)		
Size C	Document Number 411671700010		Rev 0A
Date: Wednesday, January 16, 2002		Sheet 8 of 29	

SiS301LV/CH7019

Spread Range Selection

FS0	SR0	Spreading Range	Input Frequency	Modulation Rate
1	0	+/- 1.50%	10 MHz to 20 MHz	(Fin/10)*20.83 KHz
1	1	+/- 2.50%	10 MHz to 20 MHz	(Fin/10)*20.83 KHz
0	0	+/- 1.25%	20 MHz to 35 MHz	(Fin/10)*20.83 KHz
0	1	+/- 2.00%	20 MHz to 35 MHz	(Fin/10)*20.83 KHz

FS0 and SR0 HAVE INTERNAL PULL_UP 100K Ohm

SiS301LV/ Chrontel CH7019

	VGA	YUV TV	SCART	Normal TV
GPIOA	0	0	1	1
GPIOB	0	1	0	1

GPIOC	0	0	1	1
GPIOD	0	1	0	1
Normal TV	Normal PAL	PAL-M	PAL-N	Normal NTSC
YUV TV	525I	525P	750P	1080I

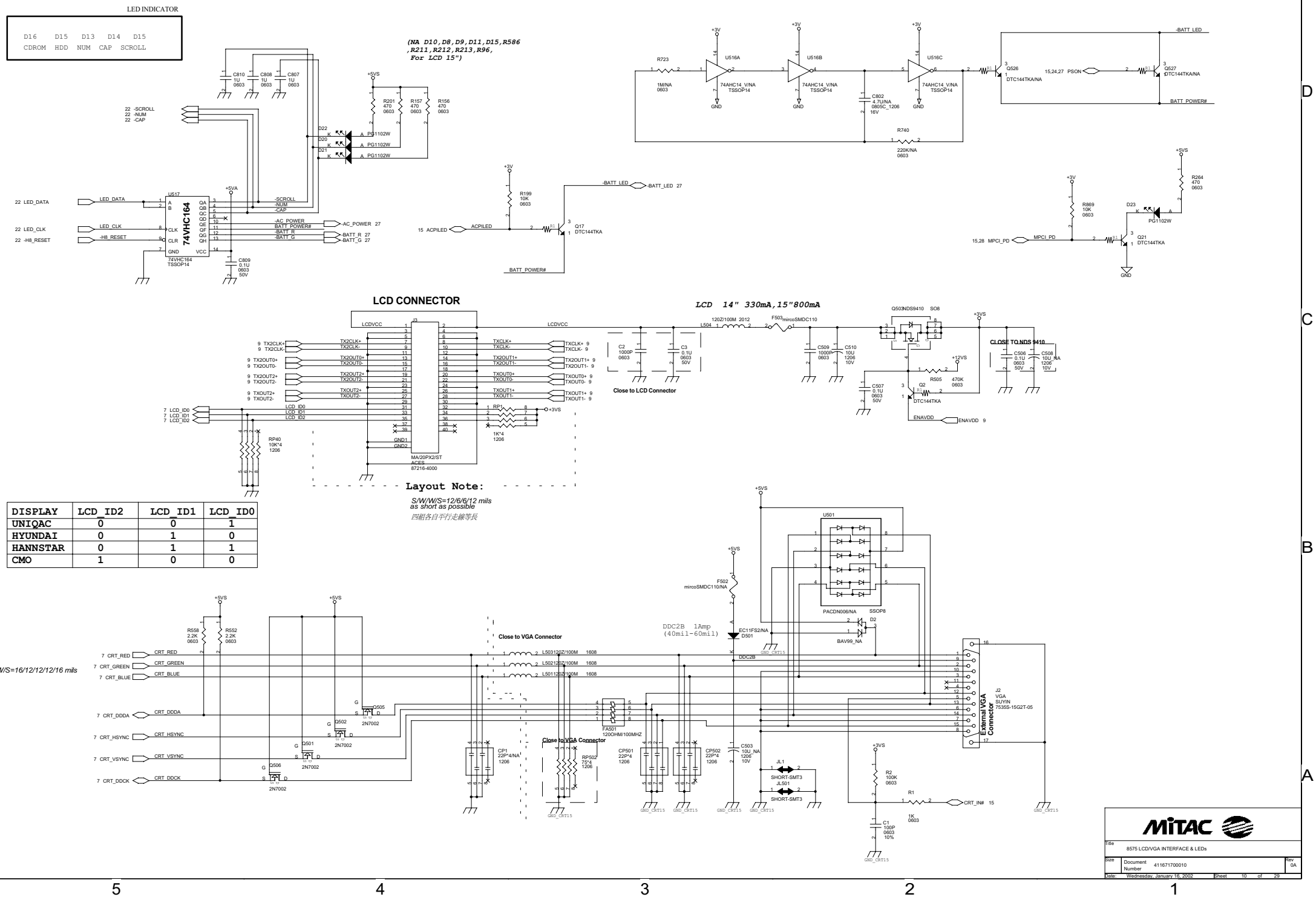
MiTAC

Title: 8575 TV/LVDS ENCODER (SiS301LV)

Size C | Document Number 411671700010 | Rev 0A

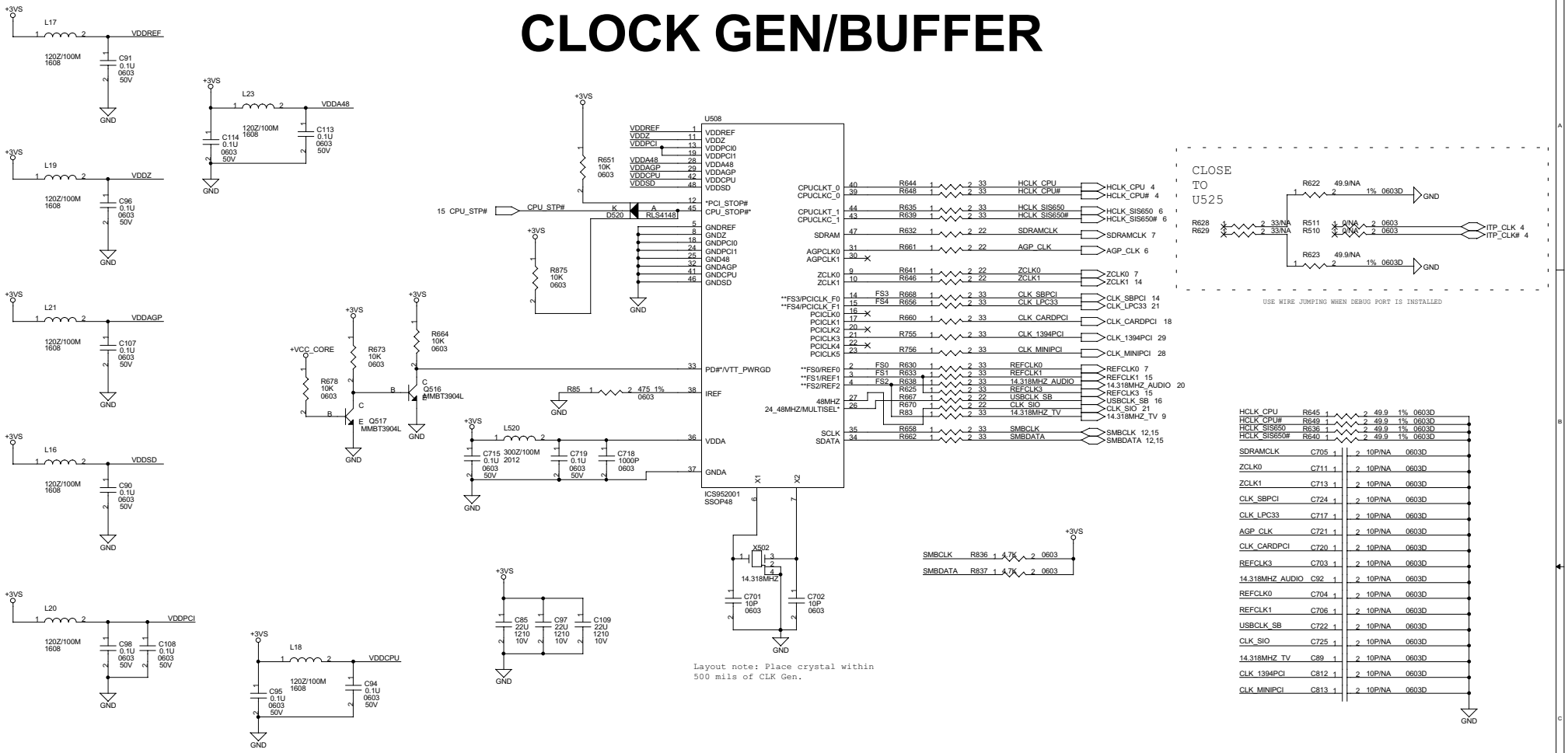
Date: Wednesday, January 16, 2002 | Sheet 9 of 29

LCD & CRT INTERFACE



DISPLAY	LCD_ID2	LCD_ID1	LCD_ID0
UNIQAC	0	0	1
HYUNDAI	0	1	0
HANNSTAR	0	1	1
CMO	1	0	0

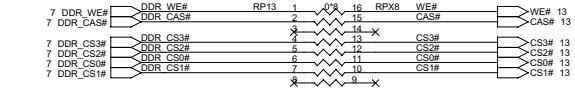
CLOCK GEN/BUFFER

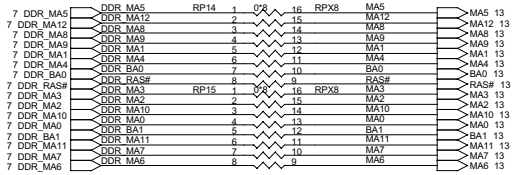


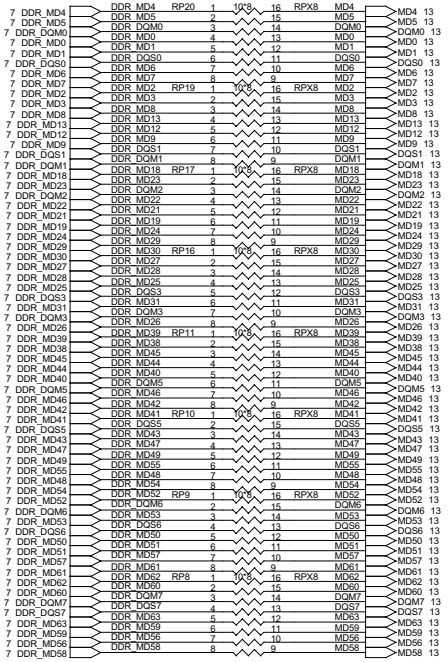
Bit 2 FS4	Bit 7 FS3	Bit 6 FS2	Bit 4 FS1	Bit 5 FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGP (MHz)
0	0	0	0	0	66.67	66.67	66.67	66.67
0	0	0	0	1	100.00	100.00	66.67	66.67
0	0	0	1	0	100.00	200.00	66.67	66.67
0	0	0	1	1	100.00	133.33	66.67	66.67
0	0	1	0	0	100.00	150.00	60.00	60.00
0	0	1	0	1	100.00	125.00	62.50	62.50
0	0	1	1	0	100.00	160.00	66.67	66.67
0	0	1	1	1	100.00	133.33	80.00	66.67
0	1	0	0	0	100.00	200.00	66.67	66.67
0	1	0	0	1	100.00	166.67	62.50	62.50
0	1	0	1	0	100.00	166.67	71.43	83.33
0	1	0	1	1	80.00	133.33	66.67	66.67
0	1	1	0	0	80.00	133.33	66.67	66.67
0	1	1	0	1	95.00	95.00	63.33	63.33
0	1	1	1	0	95.00	126.67	63.33	63.33
0	1	1	1	1	66.67	66.67	50.00	50.00

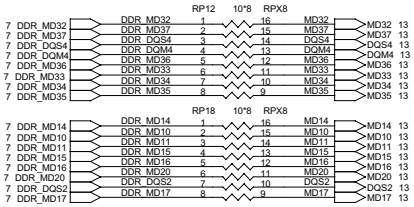
Title	8575 MAIN CLOCK & CLOCK BUFFER
Size C	Document Number 411671700010 Rev 0A
Date: Wednesday, January 16, 2002	Sheet 11 of 29

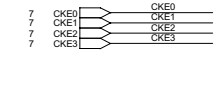
DDR SODIMM

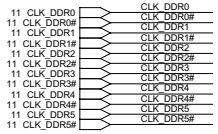


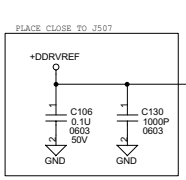


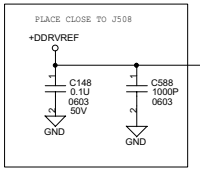


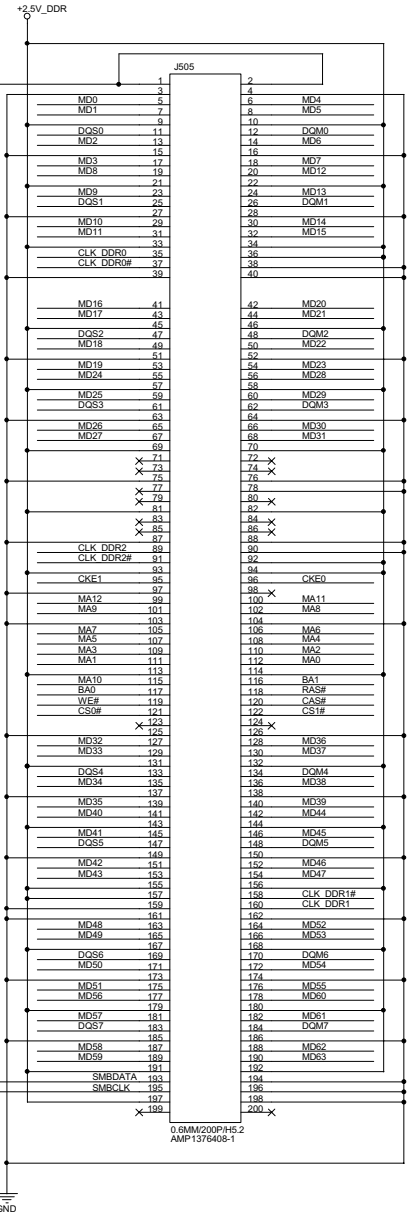


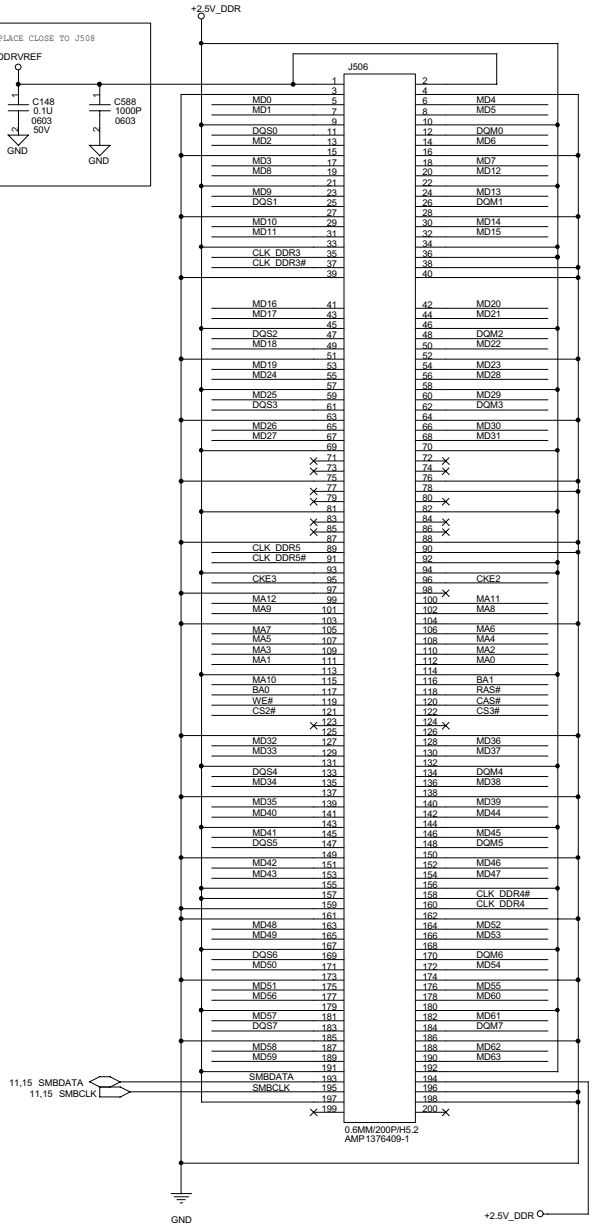


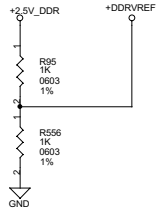


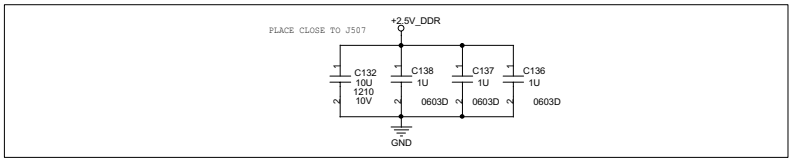


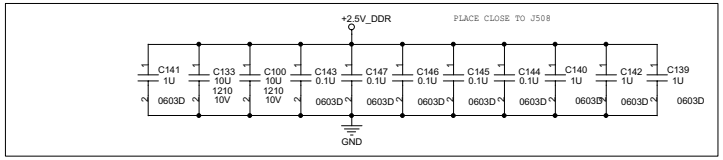










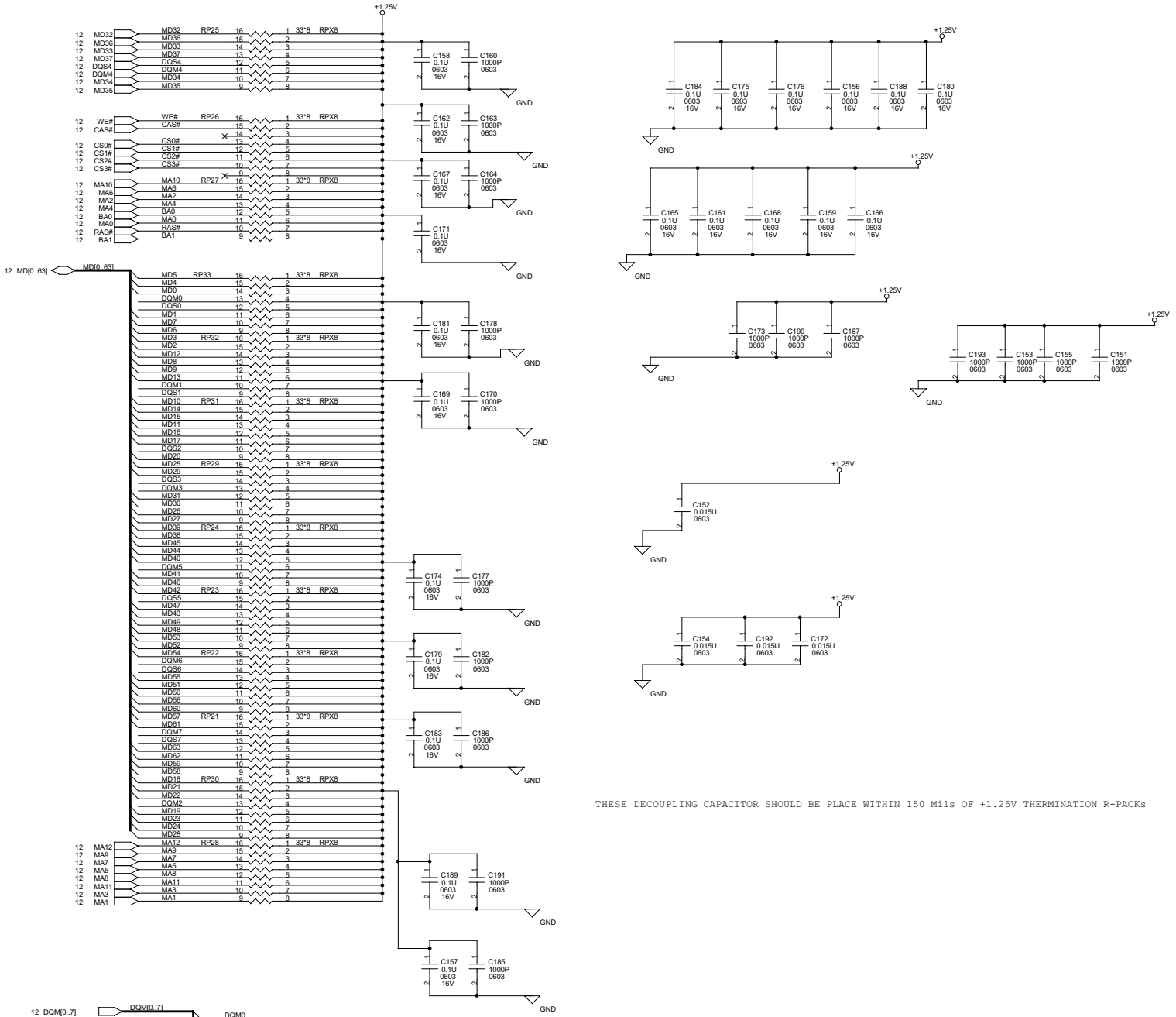


MiTAC

Title: 8575 DDR SO-DIMMs

Size	Document Number	Rev
C	411671700010	0A

Date: Wednesday, January 16, 2002 Sheet 12 of 29

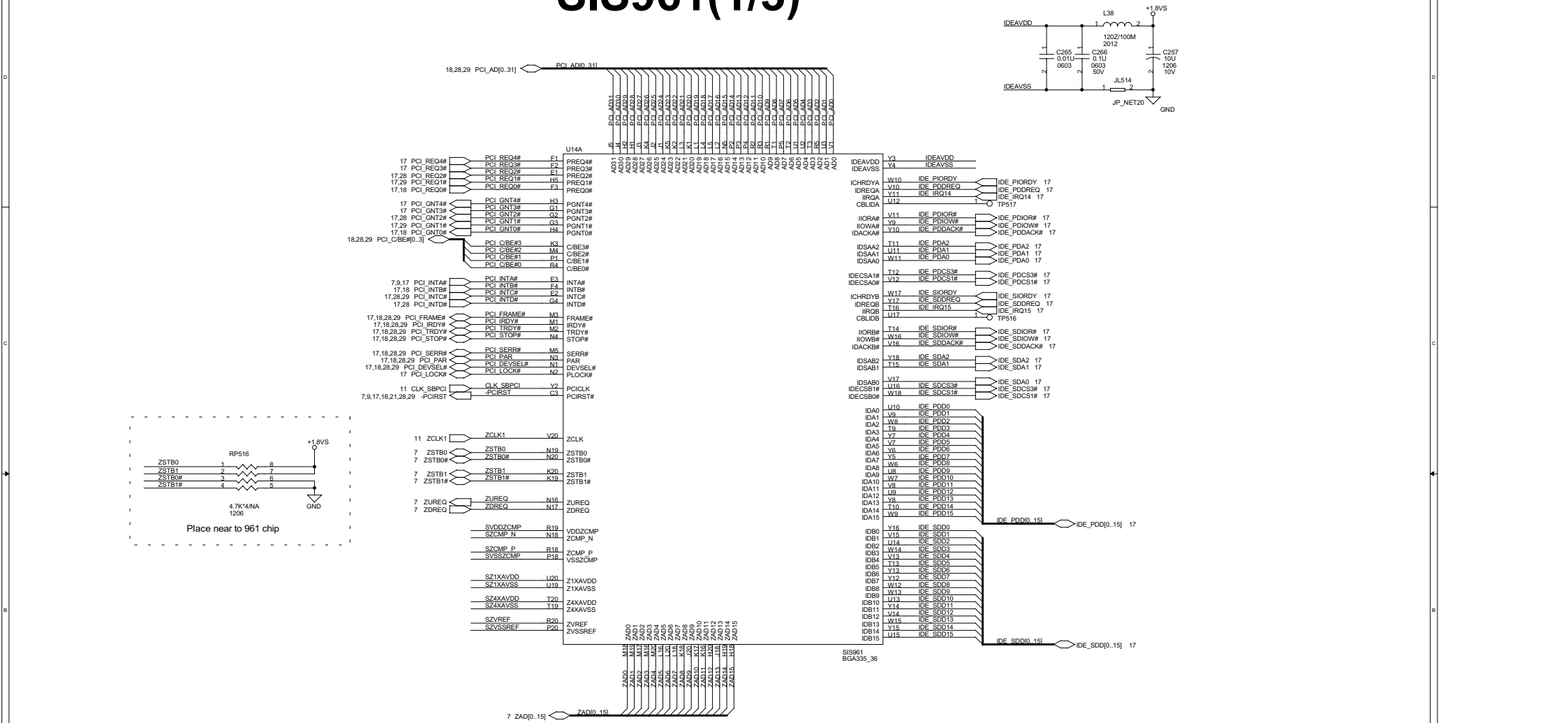


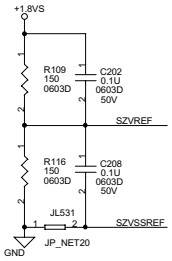
THESE DECOUPLING CAPACITOR SHOULD BE PLACE WITHIN 150 Mils OF +1.25V THERMINATION R-PACKs

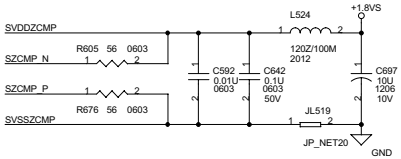
MiTAC

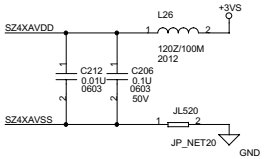
Title	8575 DDR TERMINATION	
Size C	Document Number 411671700010	Rev 0A
Date: Wednesday, January 16, 2002	Sheet 13 of 29	

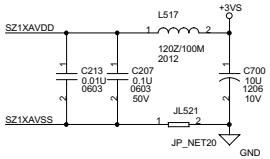
SIS961(1/3)





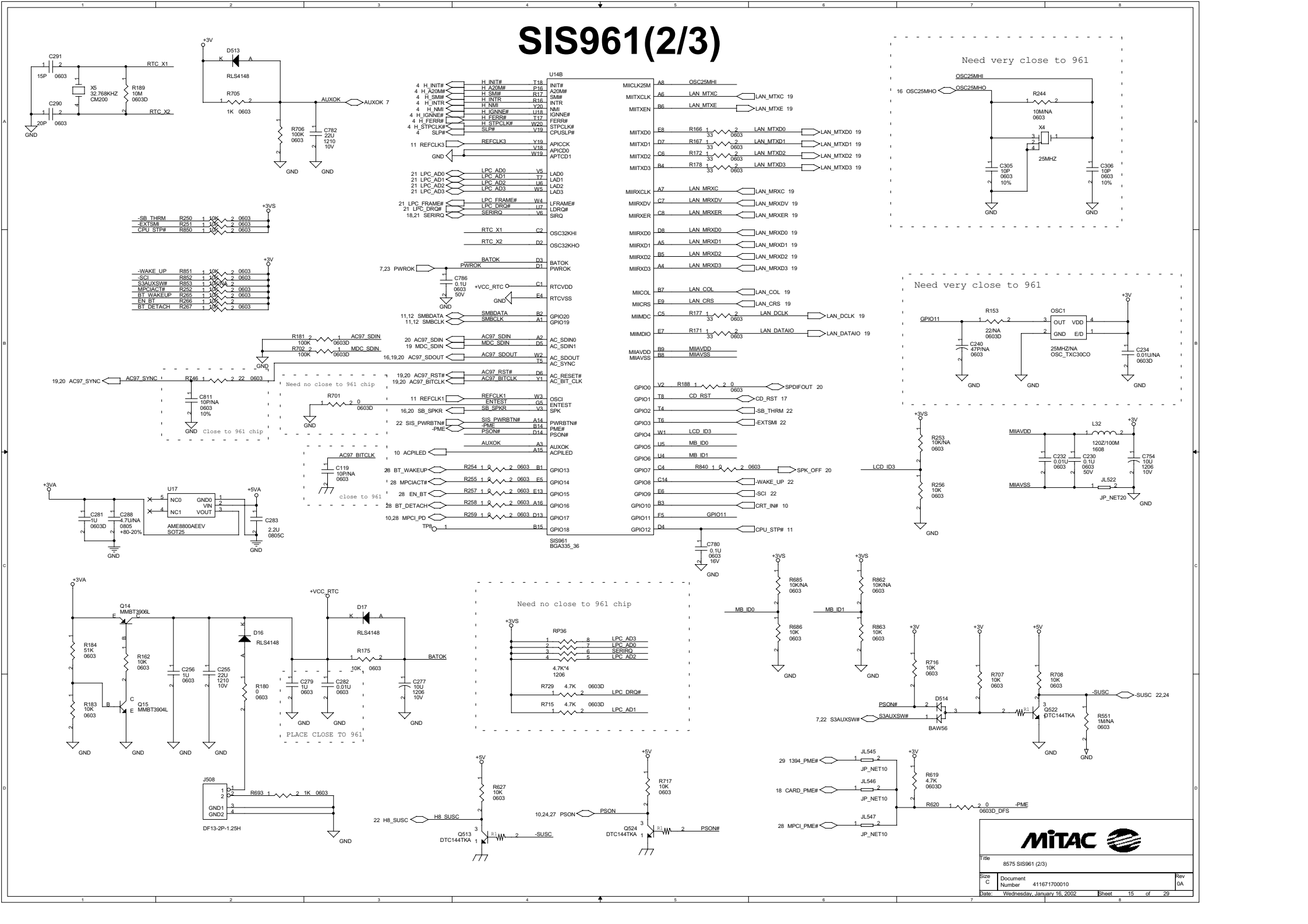




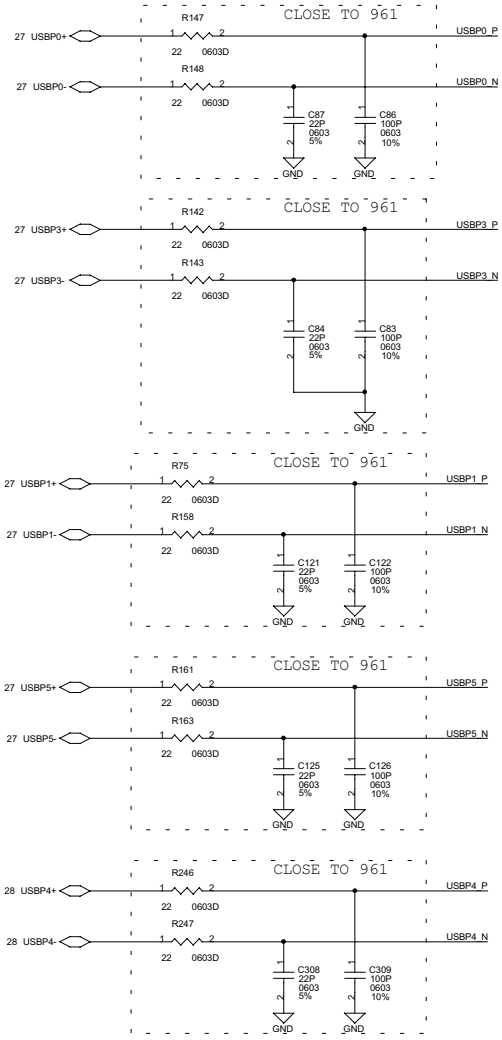


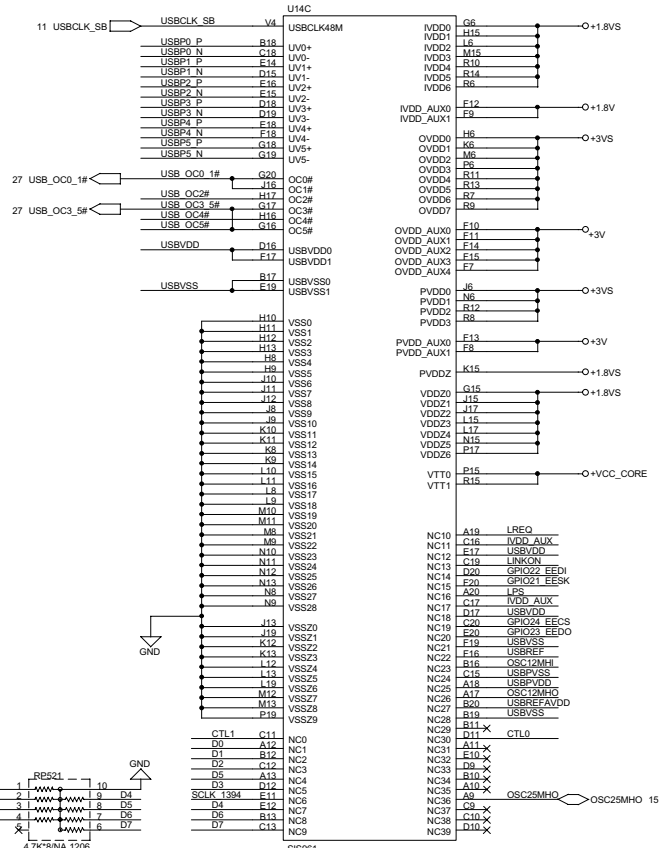
MiTAC			
Title	8575 SIS961 (1/3)		
Size C	Document Number 411671700010		Rev 0A
Date: Wednesday, January 16, 2002	Sheet 14 of 29		

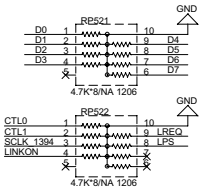
SIS961(2/3)

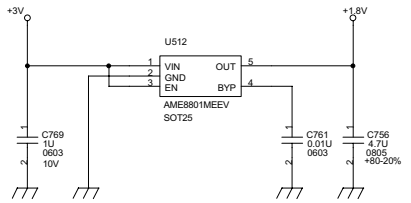

Need very close to 961
Need very close to 961
Need no close to 961 chip
Close to 961 chip
close to 961
PLACE CLOSE TO 961
U14B
SIS961
BGA335_36
U17
AME8800AEEV
SOT25
J508
DF13-2P-1.25H
Title
8575 SIS961 (2/3)
Size C
Document Number 411671700010
Rev 0A
Date: Wednesday, January 16, 2002
Sheet 15 of 29

SIS961(3/3)

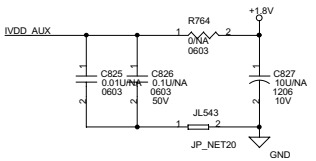


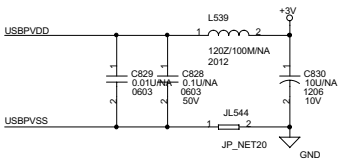


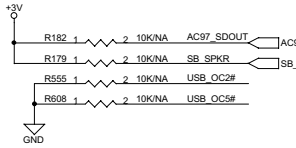


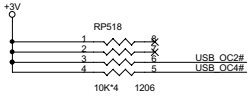


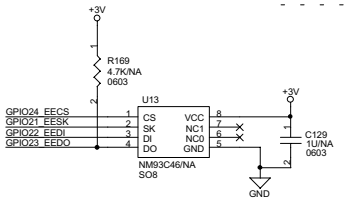
	0	1	Default
SB_SPKR (LPC addr mapping)	disable	enable	0
AC97_SDOUT (PCICLK PLL)	enable	disable	0
USB_OC2# (SB debug mode)	enable	disable	1
USB_OC5# (Trap mode)	PCI AD	ROM	1

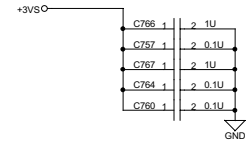


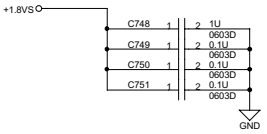


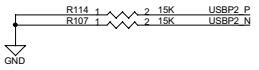


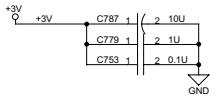


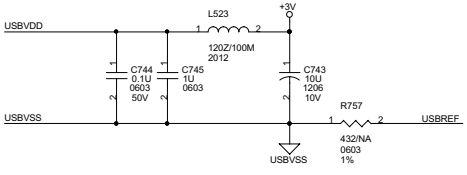


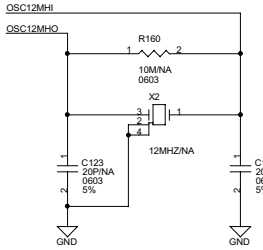


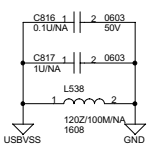


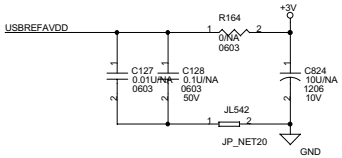


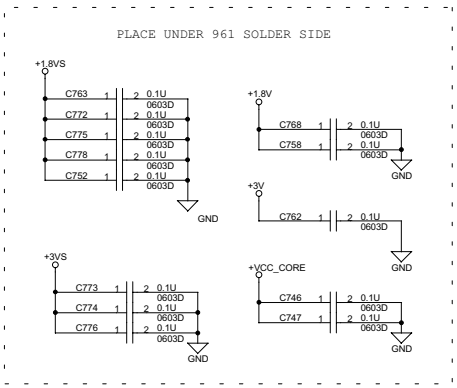












MiTAC

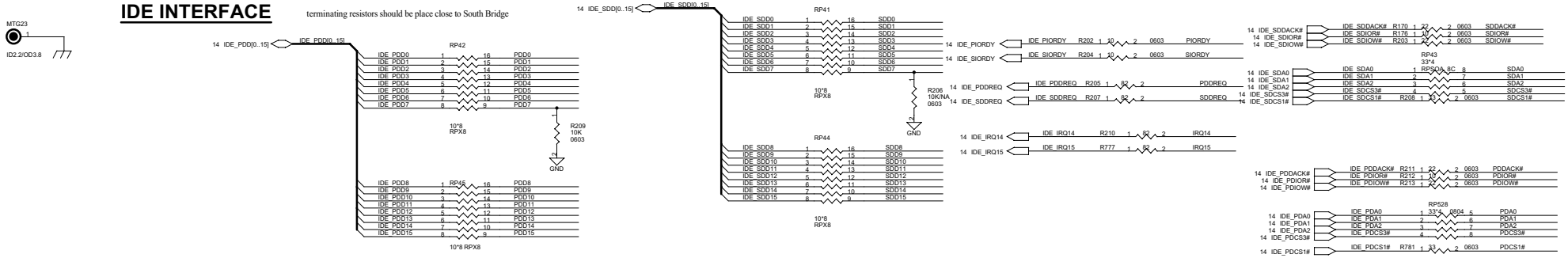
Title
8575 SIS961 (3/3)

Size C
Document Number 411671700010
Rev 0A

Date: Wednesday, January 16, 2002
Sheet 16 of 29

IDE INTERFACE

terminating resistors should be place close to South Bridge



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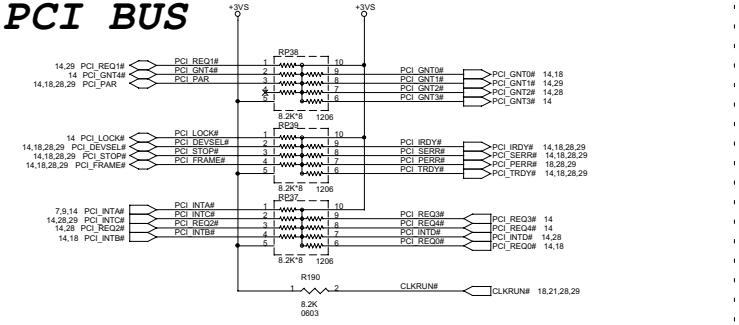
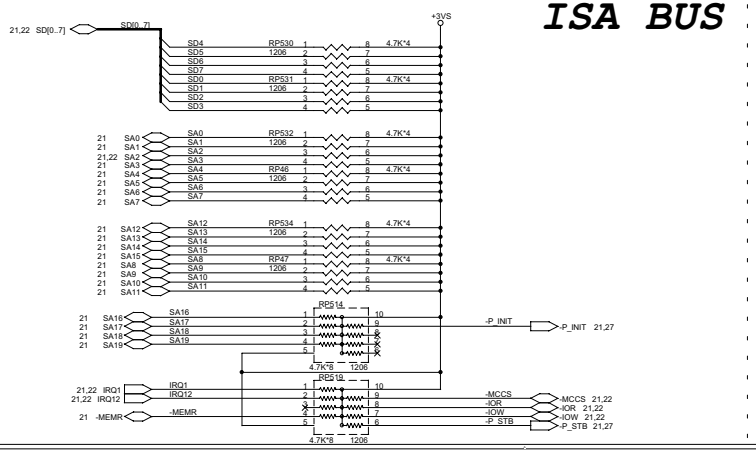
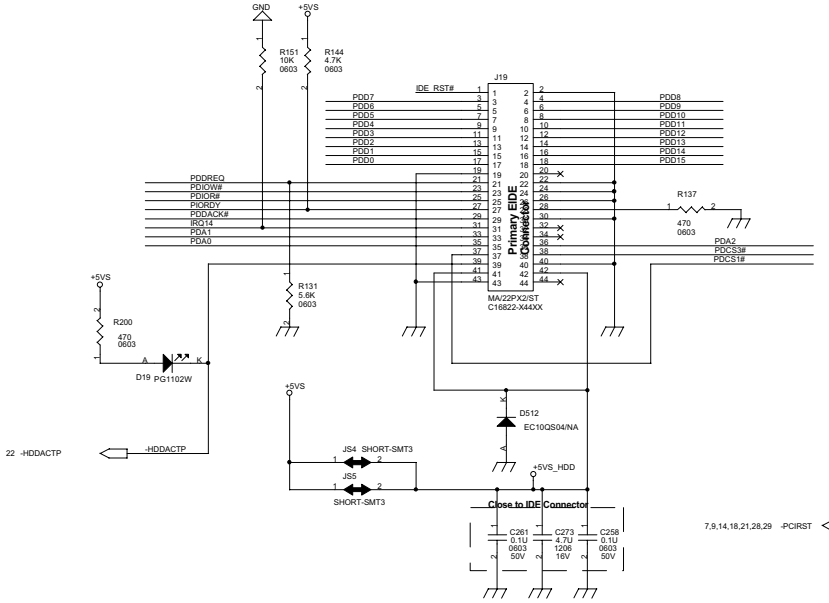
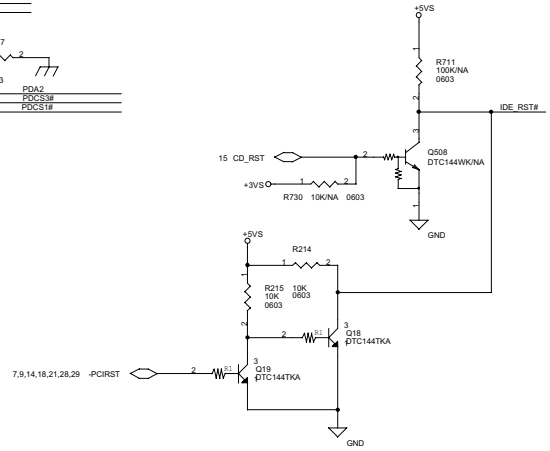
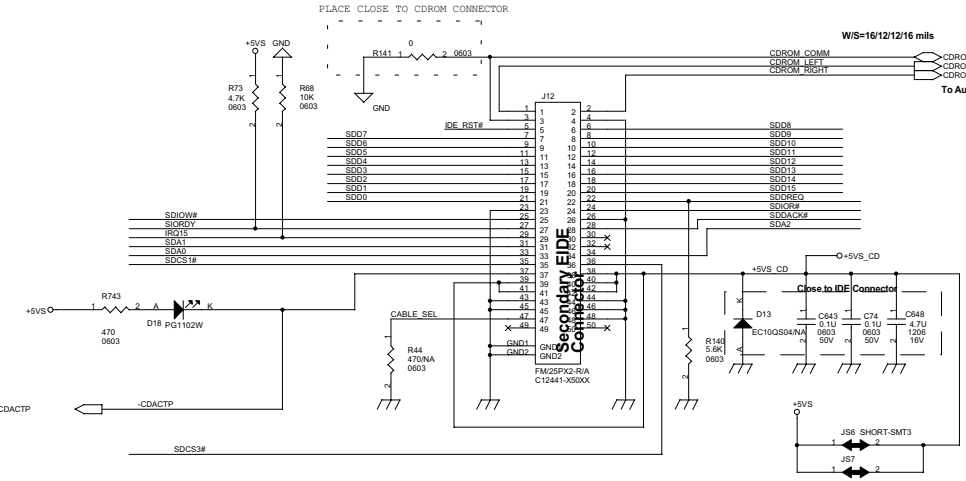


ISA BUS









Title	8575 IDE INTERFACE & PULL-UPs		
Size C	Document Number 411671700010		Rev 0A
Date: Wednesday, January 16, 2002	Sheet 17 of 29		

PCMCIA CONTROLLER & CARDBUS SCOKET

PCI1410

AD20

PCI_INTB#

REQ0#/GNT0#

FOR TI 1410

SIGNAL	PC CARD PULL UP	VOLT
CCD#1	+3V	
CCD#2	+3V	
CBLOCK#	CARD_VCC	
CSTOP#	CARD_VCC	
CDEVSEL#	CARD_VCC	
CTRDY#	CARD_VCC	
CVS1	+3V	
CVS2	+3V	
CRST#	CARD_VCC	
CSERR#	CARD_VCC	
CPERR#	CARD_VCC	
CINT#	CARD_VCC	
CIRDY#	CARD_VCC	
CREQ#	CARD_VCC	
CSTSCHG#	CARD_VCC	
CAUDIO	CARD_VCC	

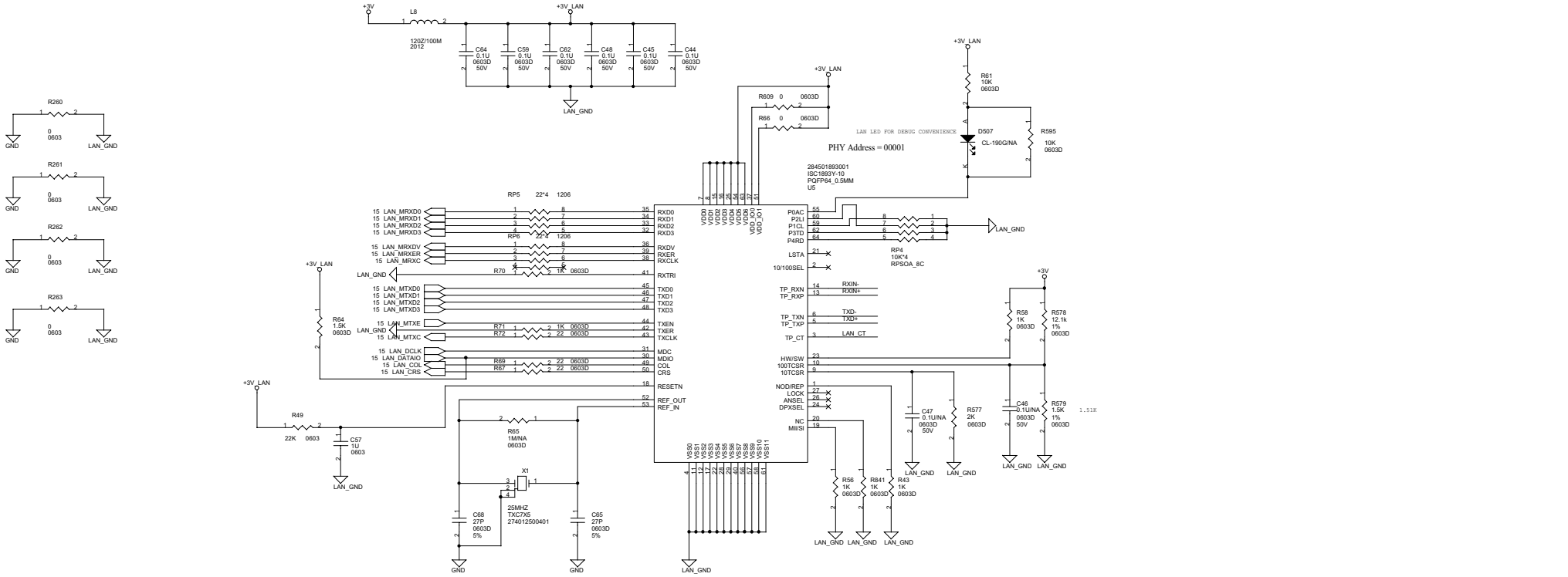
PCI1410 HAVE INTEGRATED ALL PULL UP RES ABOVE

Card Bus Socket

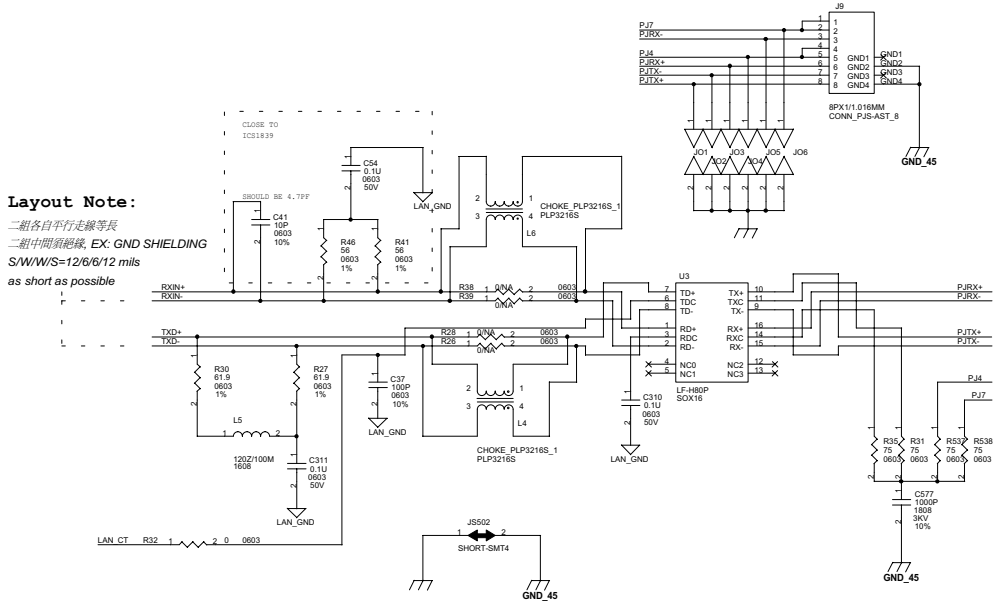
Close to TPS2211

Close to TPS2211

Title	8575 PCI1410 & CARDBUS SOCKET
Size	Document Number 411671700010 — Rev 0A
Date:	Wednesday, January 16, 2002 — Sheet 18 of 29



RJ45



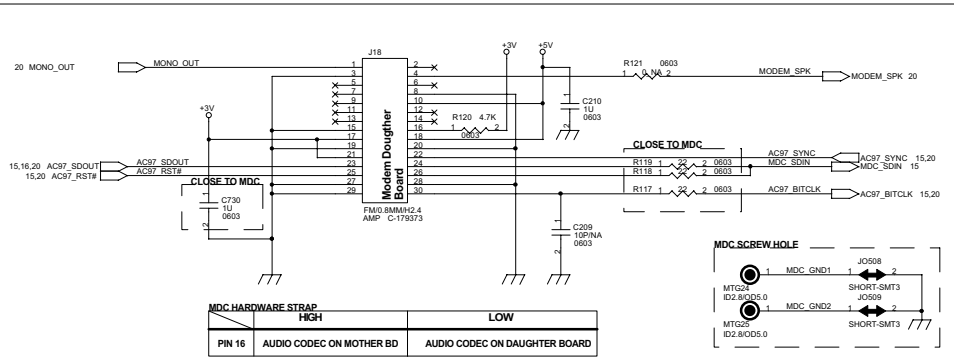
Layout Note:

二組各自平行走線等長

二組中間須絕緣, EX: GND SHIELDING

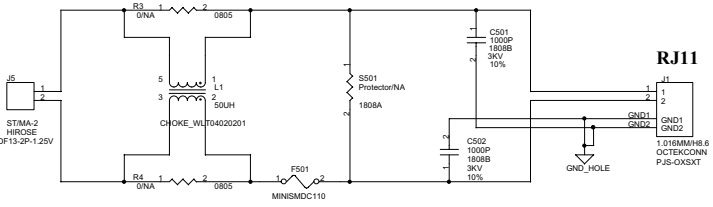
S/W/W/S=12/6/6/12 mils

as short as possible



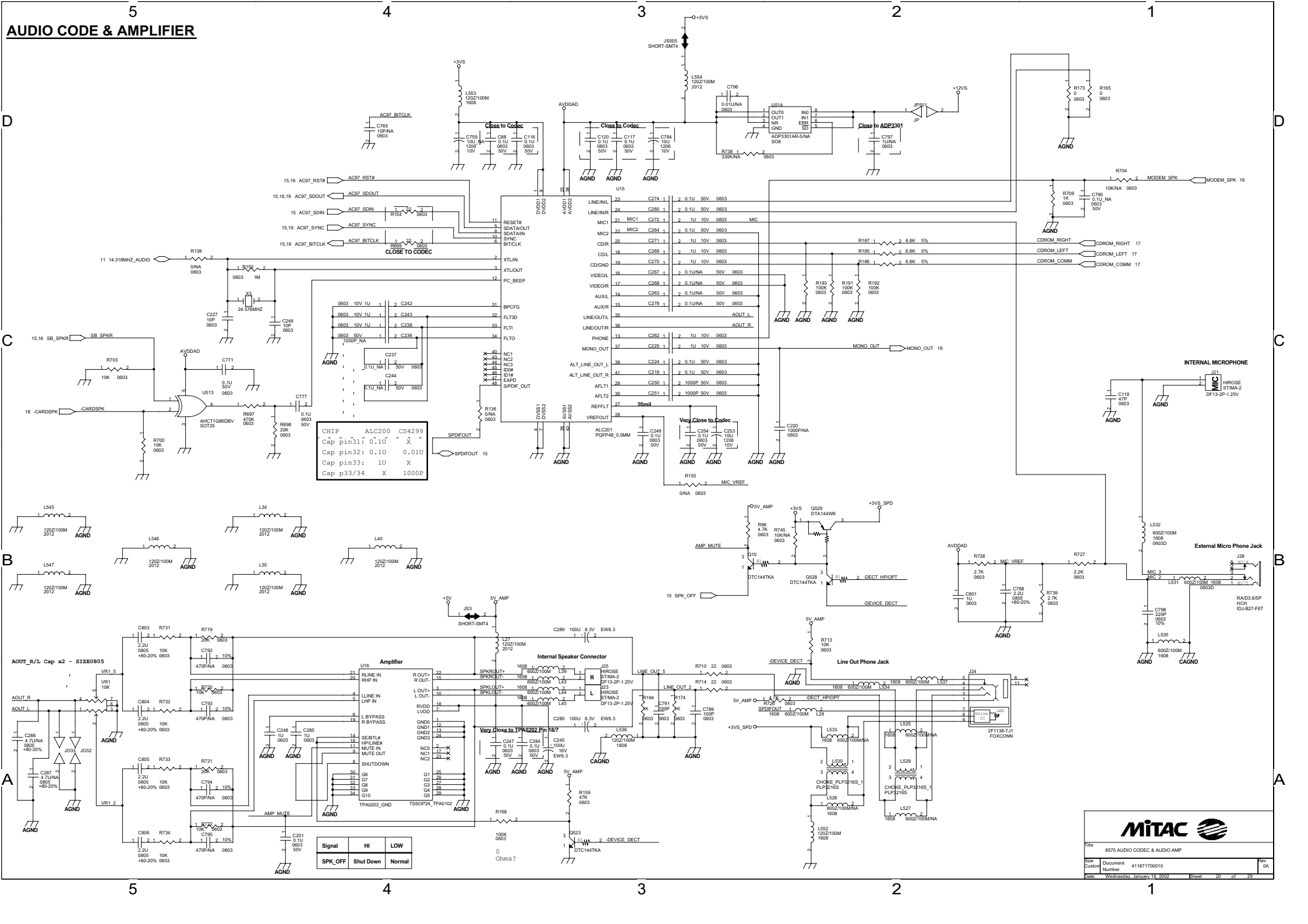
MDC HARDWARE STRAP	HIGH	LOW
PIN 16	AUDIO CODEC ON MOTHER BD	AUDIO CODEC ON DAUGHTER BOARD

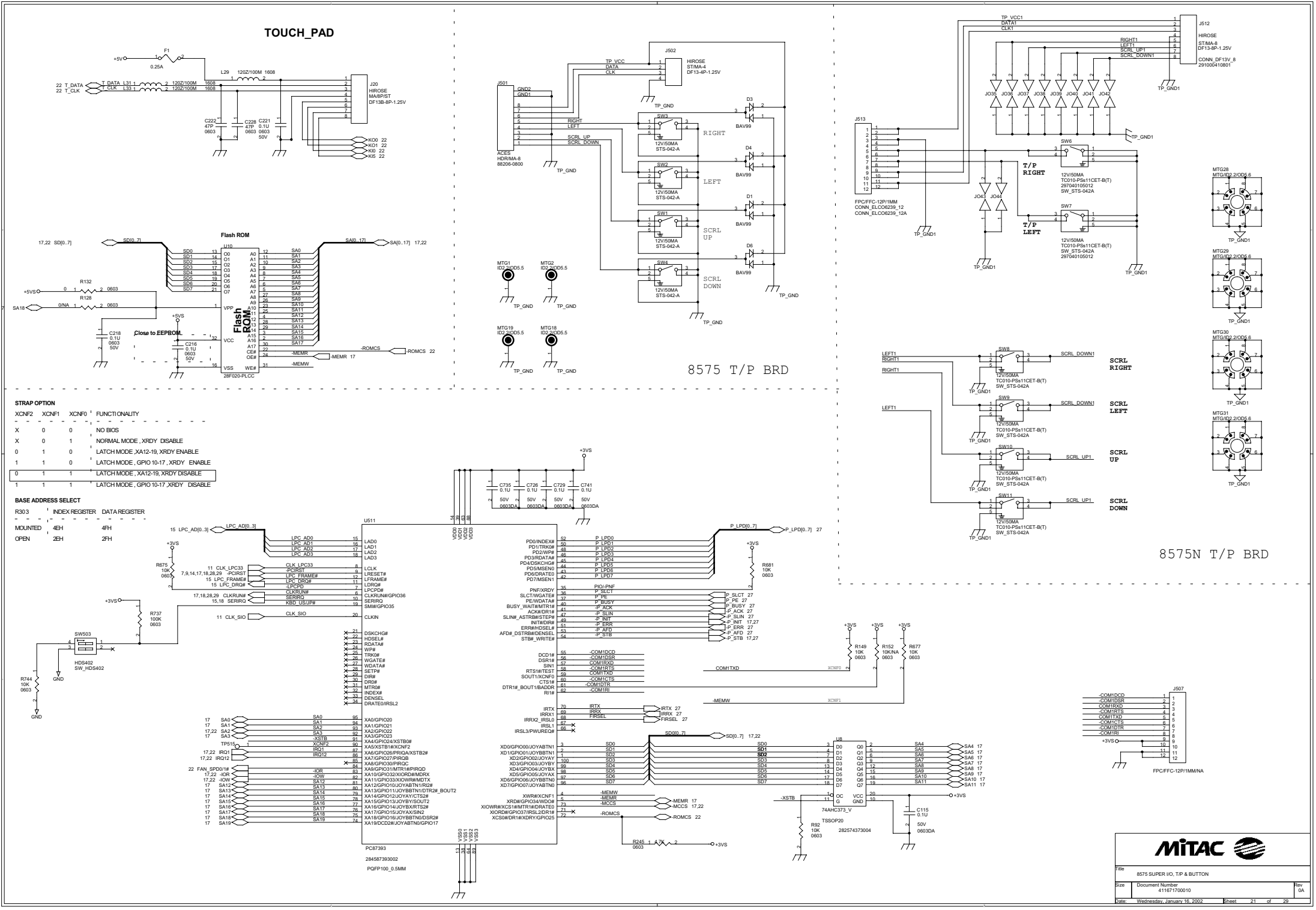
RJ11



Title	8575 LAN PHY (ICS1893) & MDC
Size: Custom	Document Number: 411671700010
Rev	0A
Date:	Wednesday, January 16, 2002 Sheet 19 of 29

AUDIO CODE & AMPLIFIER




TOUCH_PAD
Flash ROM
Close to EEPROM.
28F020-PLCC
8575 T/P BRD
8575N T/P BRD
STRAP OPTION
XCNF2 XCNF1 XCNF0 FUNCTIONALITY
X 0 0 NO BIOS
X 0 1 NORMAL MODE , XRDY DISABLE
0 1 0 LATCH MODE ,XA12-19, XRDY ENABLE
1 1 0 LATCH MODE , GPIO 10-17 , XRDY ENABLE
0 1 1 LATCH MODE , XA12-19, XRDY DISABLE
1 1 1 LATCH MODE , GPIO 10-17 ,XRDY DISABLE
BASE ADDRESS SELECT
R303 INDEX REGISTER DATA REGISTER
MOUNTED 4EH 4FH
OPEN 2EH 2FH
PC87393
284587393002
PQFP100_0.5MM
FPC/FFC-12P/1MM/NA
MiTAC
8575 SUPER I/O, T/P & BUTTON
Document Number 411671700010
Rev 0A
Wednesday, January 16, 2002
Sheet 21 of 29

MICROCONTROLLER (H8)

H8 Mode Select Table

MD0	MD1	MODE	Description
0	1	MODE1	Expended mode with On-Chip ROM disable
1	0	MODE2	Expended mode with On-Chip ROM enable
1	1	MODE3	Single-Chip mode

DEFAULT SHORT

Quick Switch Button: Stuff RP589, R1359
LED: Stuff RP590, R1360

NA WHILE ASSEMBLY

SECOND POWER SWITCH

Signal	HI	LOW
-LID	Normal	Suspend

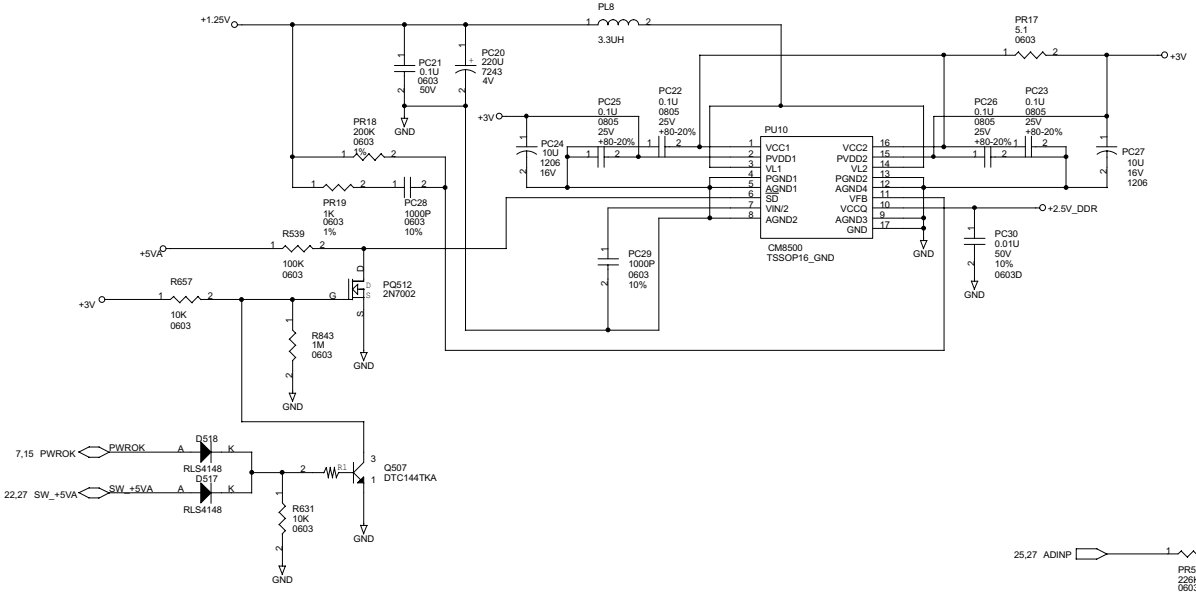
Signal	HI	LOW
-FAN	FAN Off	FAN On

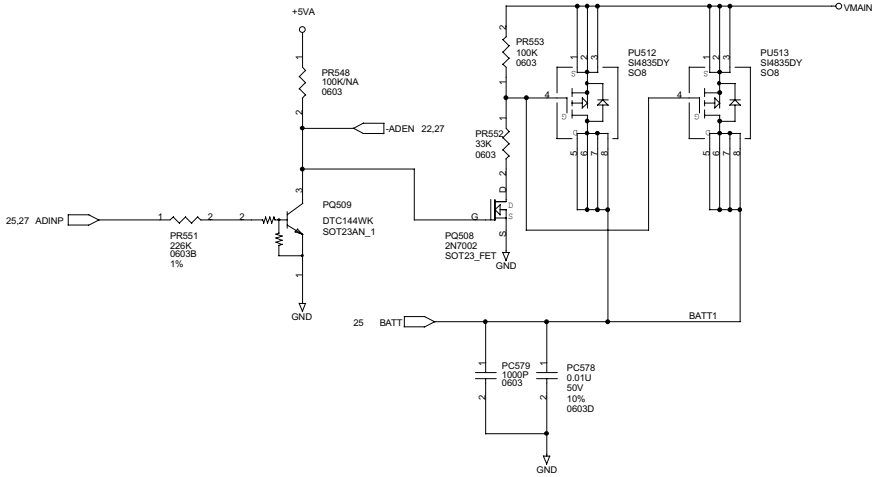
Signal	HI	LOW
-DC/DC_FAN	FAN Off	FAN On

MiTAC

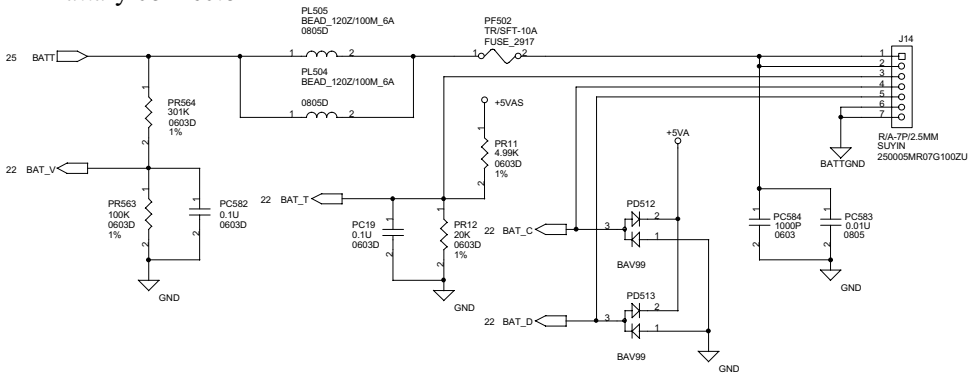
Title	8575 MICROCONTROLLER (H8)	
Size	Document Number 411671700010	Rev 0A
Date: Wednesday, January 16, 2002	Sheet 22 of 29	

1.25V CM8500 & BATTERY CONNECTOR

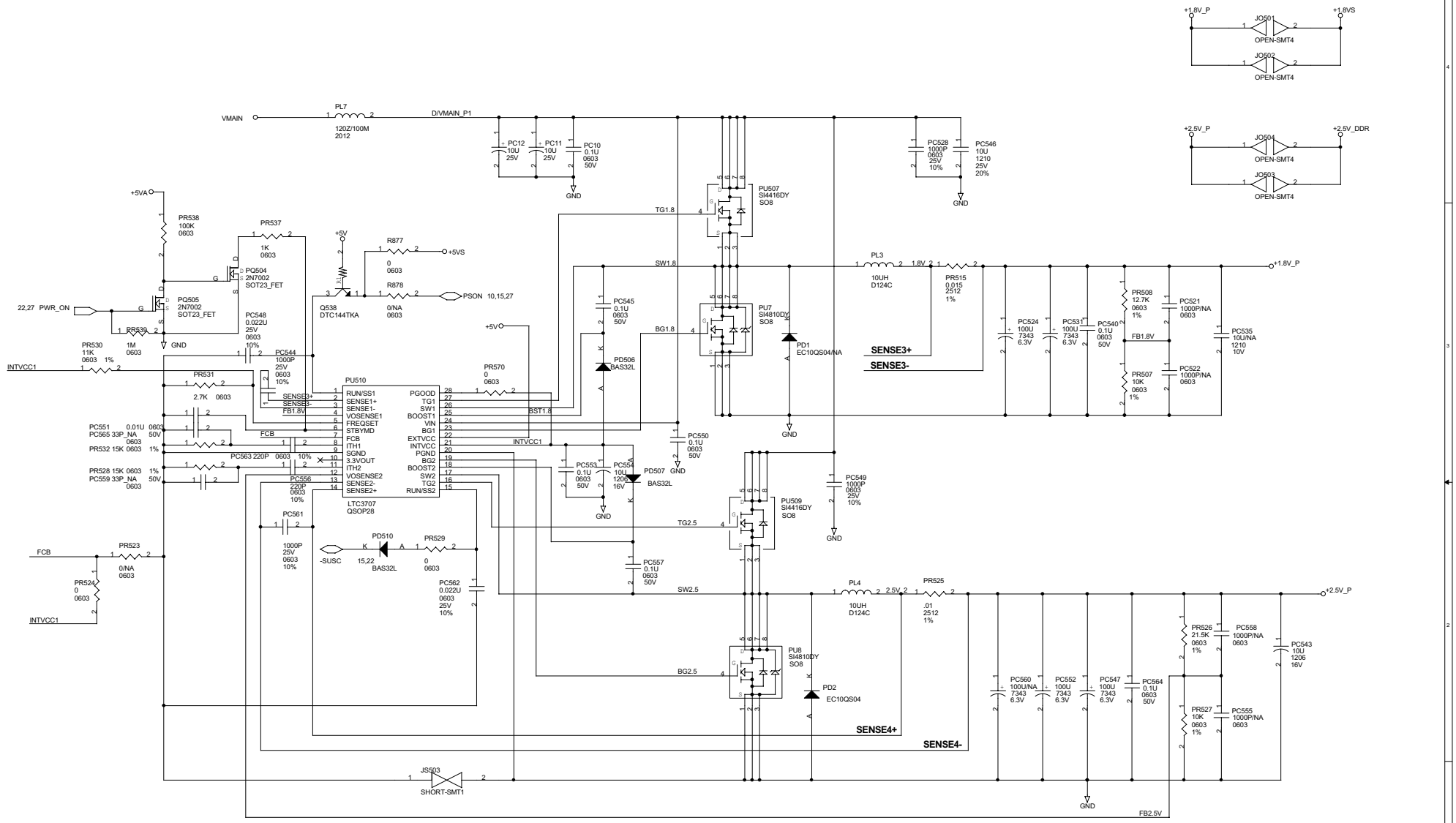




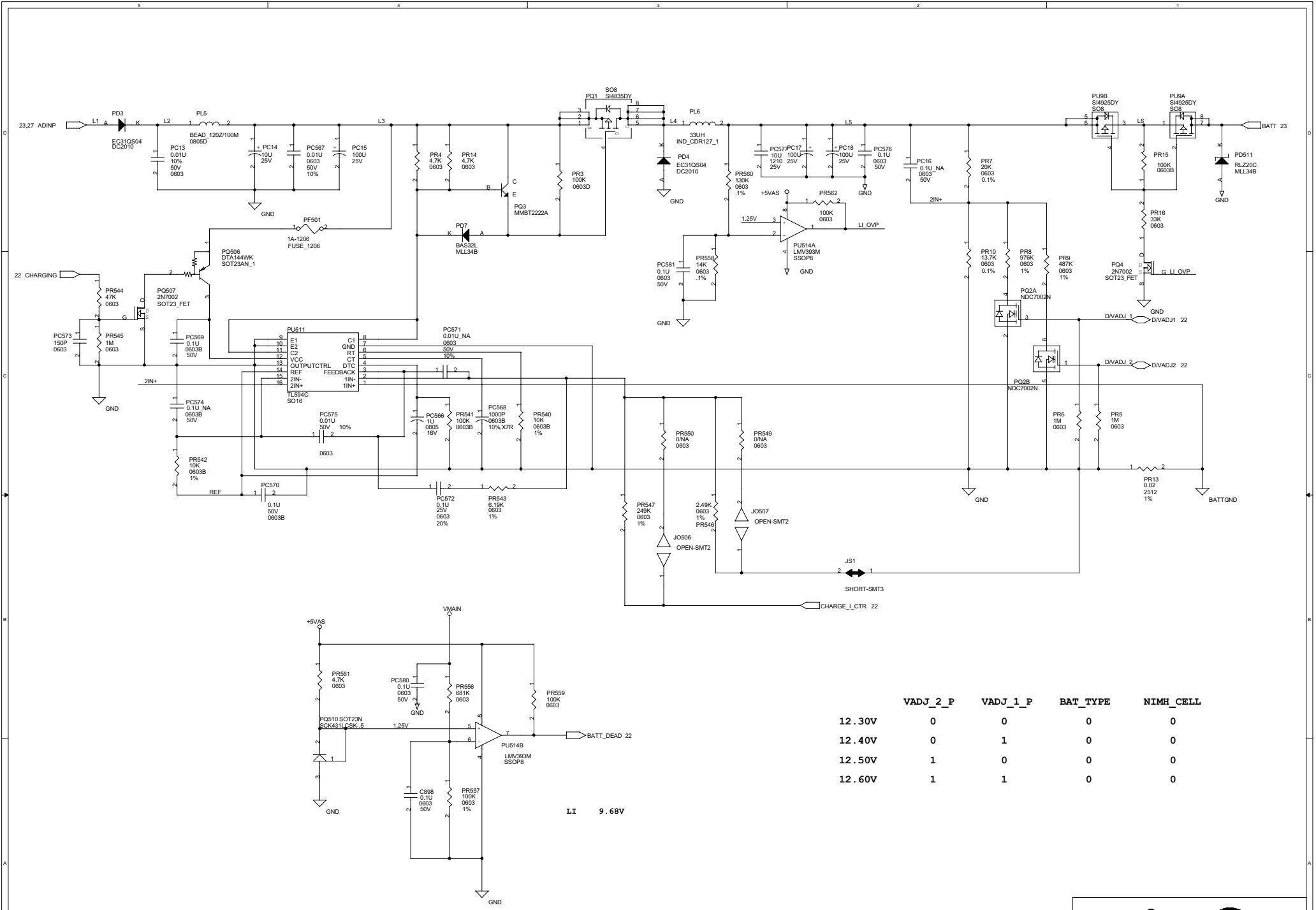
Battary connector



MiTAC			
Title	8575 1.25V PWR (CM8500) & BAT CONN		
Size C	Document Number 411671700010		Rev 0A
Date: Wednesday, January 16, 2002	Sheet 23 of 29		



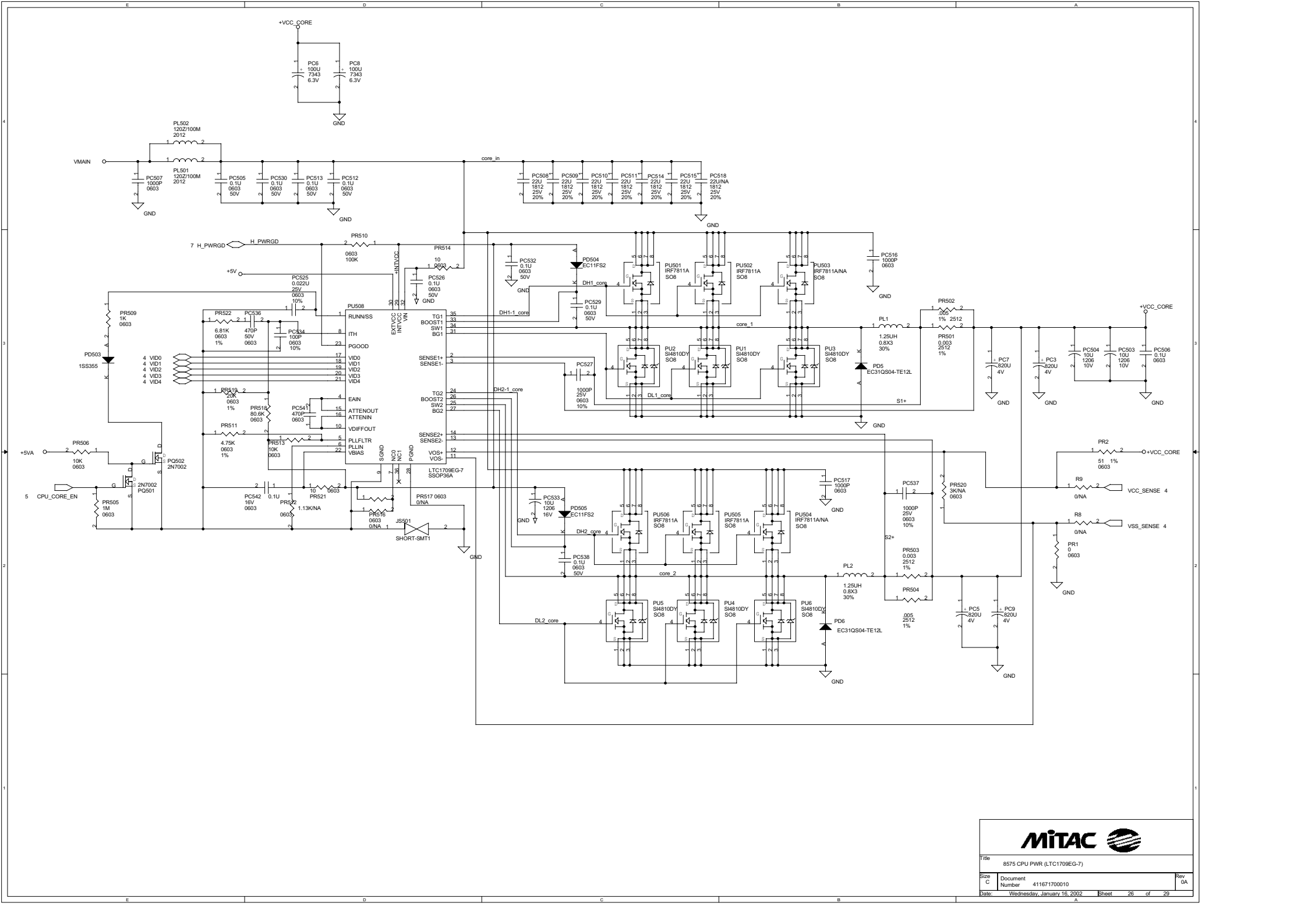
MiTAC		
Title	8575 1.8V/2.5V PWR (LTC3707)	
Size C	Document Number 411671700010	Rev 0A
Date: Wednesday, January 16, 2002	Sheet 24 of 29	



	VADJ_2_P	VADJ_1_P	BAT_TYPE	NIMH_CELL
12.30V	0	0	0	0
12.40V	0	1	0	0
12.50V	1	0	0	0
12.60V	1	1	0	0

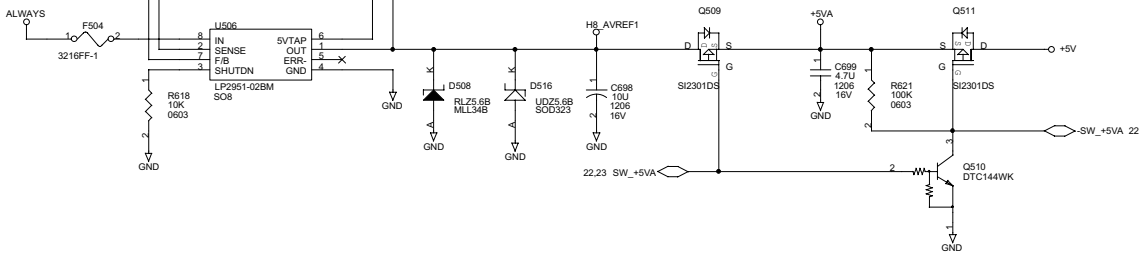
MiTAC

Title	8575 CHARGER (LT594C)	
Size C	Document Number 411671700010	Rev 0A
Date: Wednesday, January 16, 2002	Sheet 25 of 29	

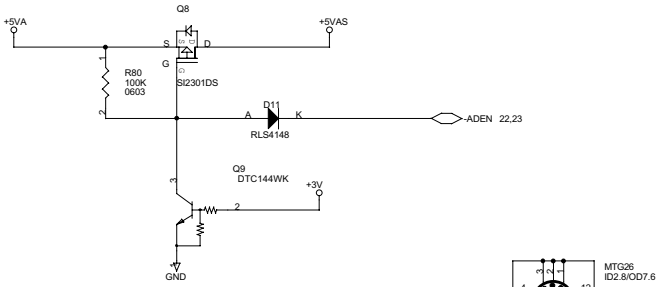


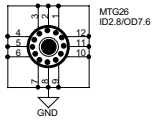
Title	8575 CPU PWR (LTC1709EG-7)	
Size C	Document Number 411671700010	Rev 0A
Date: Wednesday, January 16, 2002	Sheet 26 of 29	

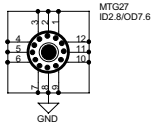
+5VA

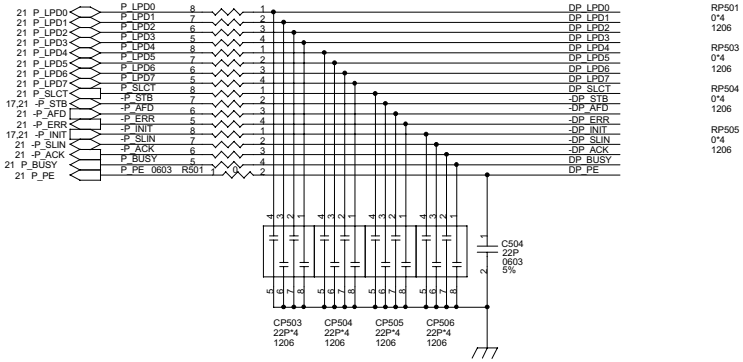


+5VAS







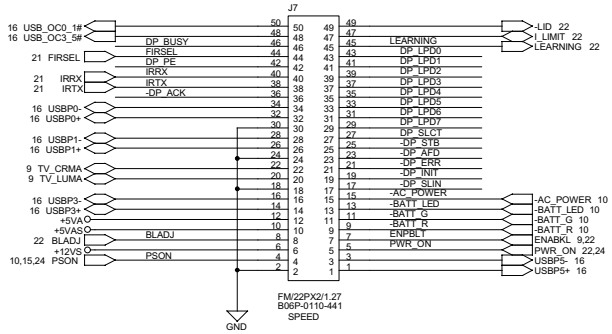


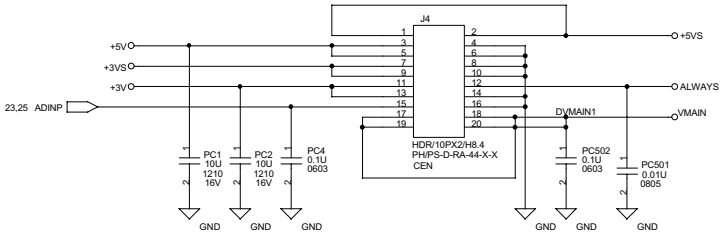
RP501
0*4
1206

RP503
0*4
1206

RP504
0*4
1206

RP505
0*4
1206



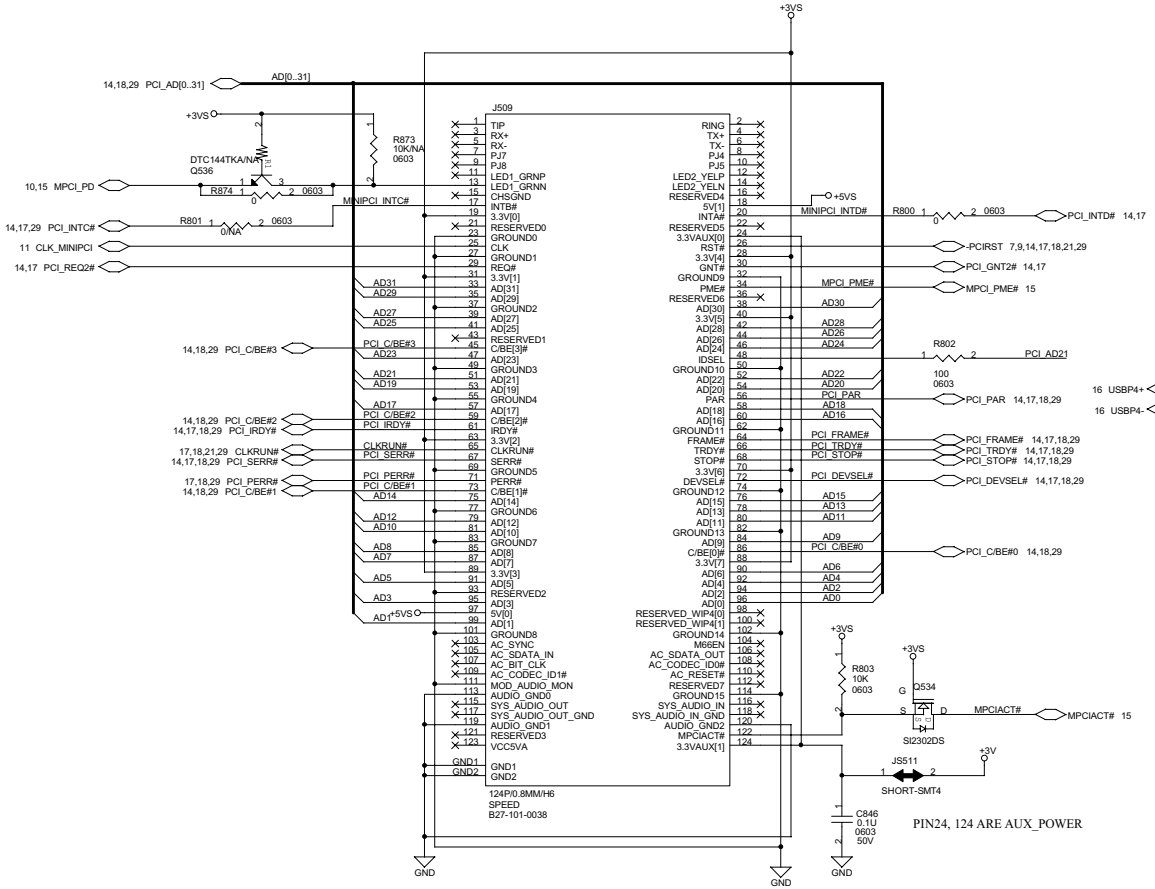


MiTAC			
Title	8575 D/D CONN & MISC		
Size C	Document Number 411671700010		Rev 0A
Date: Wednesday, January 16, 2002	Sheet 27 of 29		

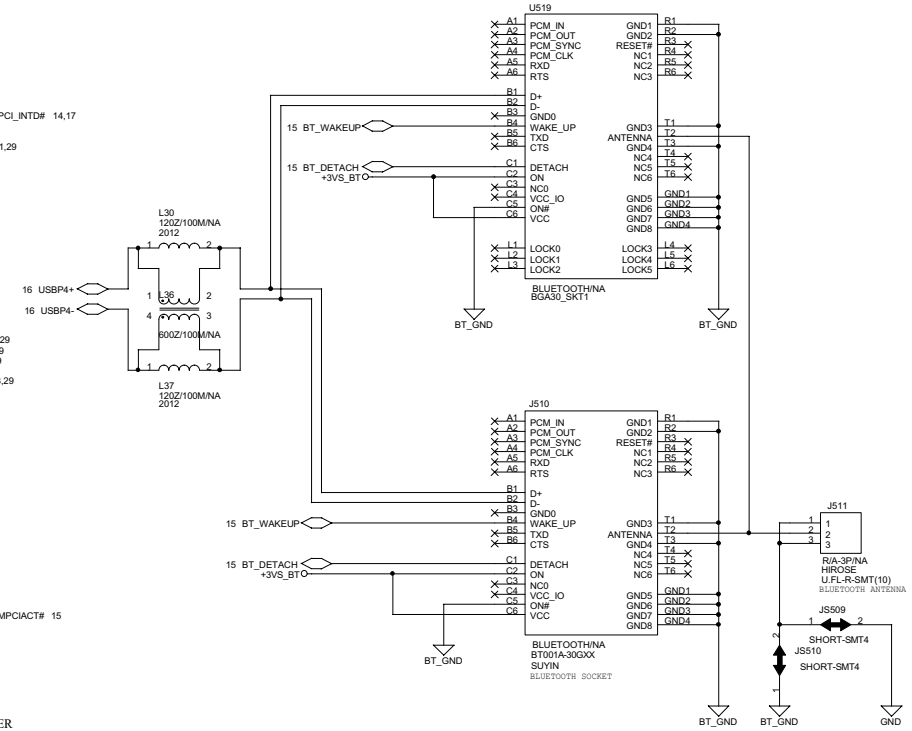
MINI-PCI & BLUETOOTH

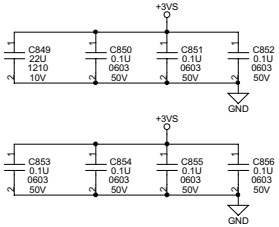
MINI-PCI

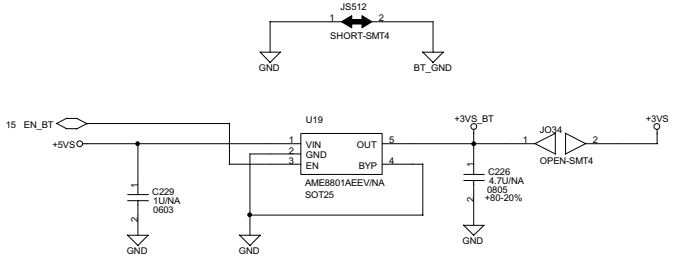
AD21
PCI_INTD#
REQ2#/GNT2#

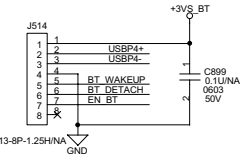


BLUETOOTH MODULE





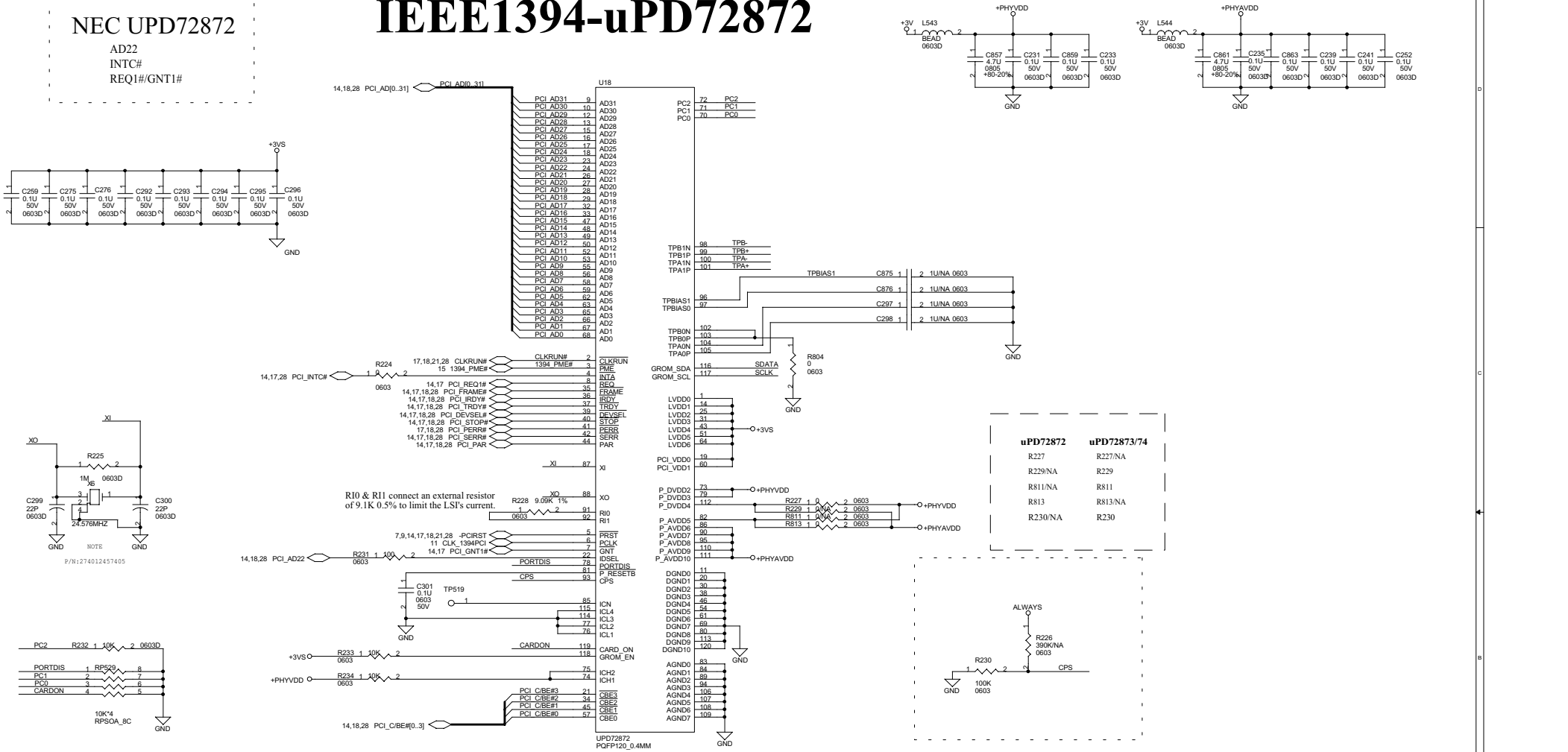




MiTAC		
Title	8575 MINIPCI & BLUETOOTH	
Size C	Document Number 411671700010	Rev 0A
Date: Wednesday, January 16, 2002	Sheet 28 of 29	

IEEE1394-uPD72872

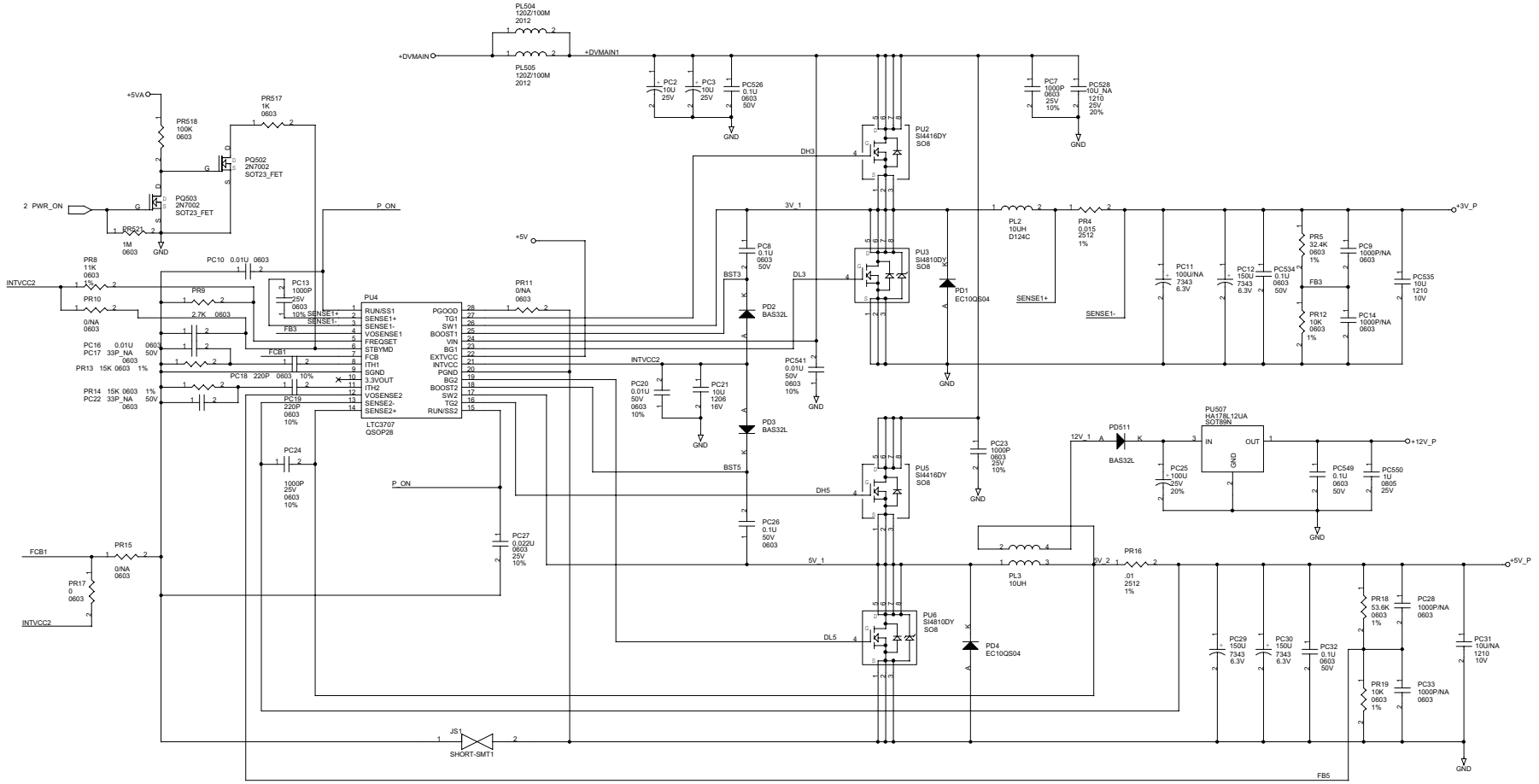
NEC UPD72872
AD22
INTC#
REQ1#/GNT1#



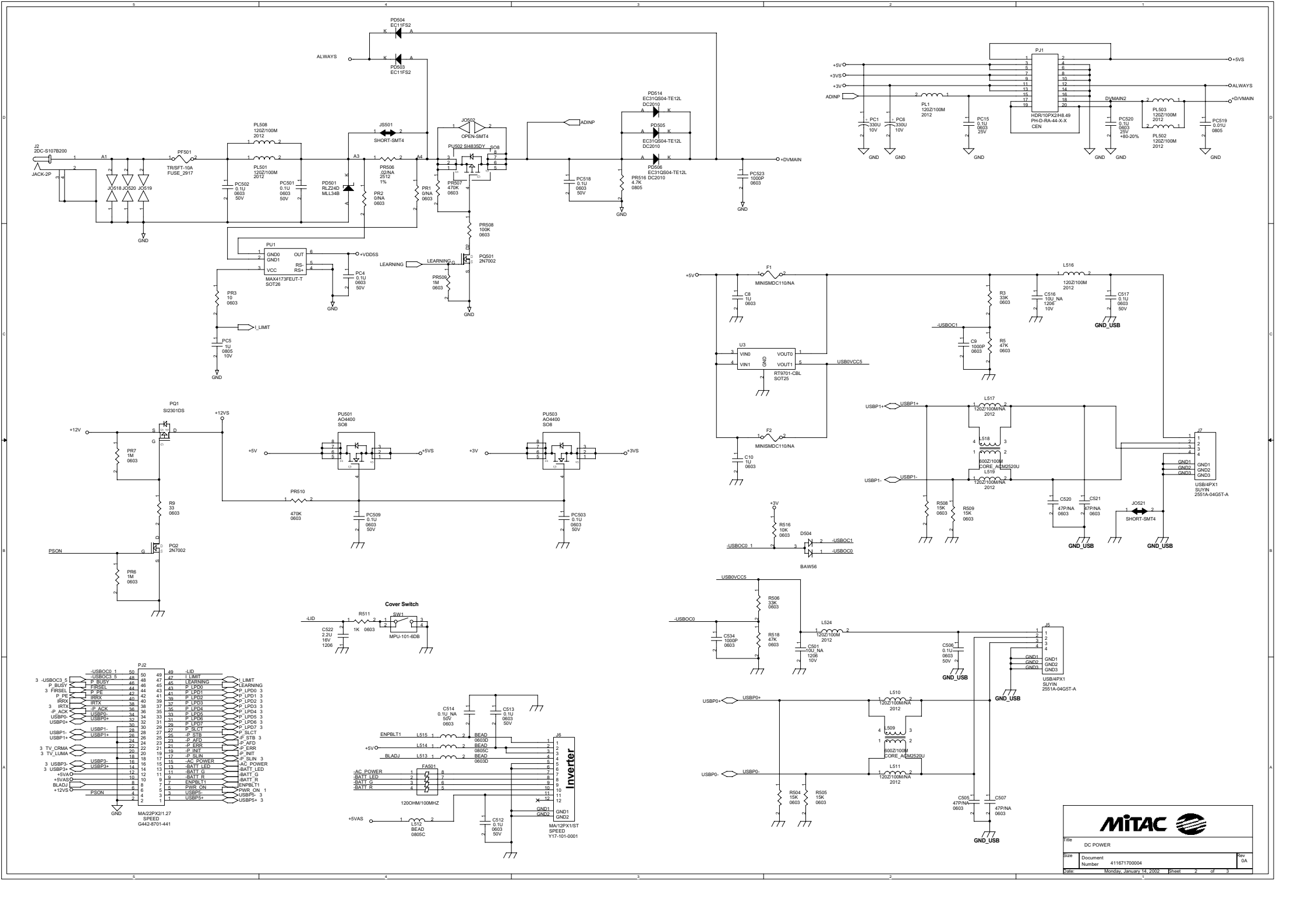
Title	8575 IEEE1394 (uPD72872)
Size	C
Document Number	411671700010
Rev	0A
Date:	Wednesday, January 16, 2002
Sheet	29 of 29

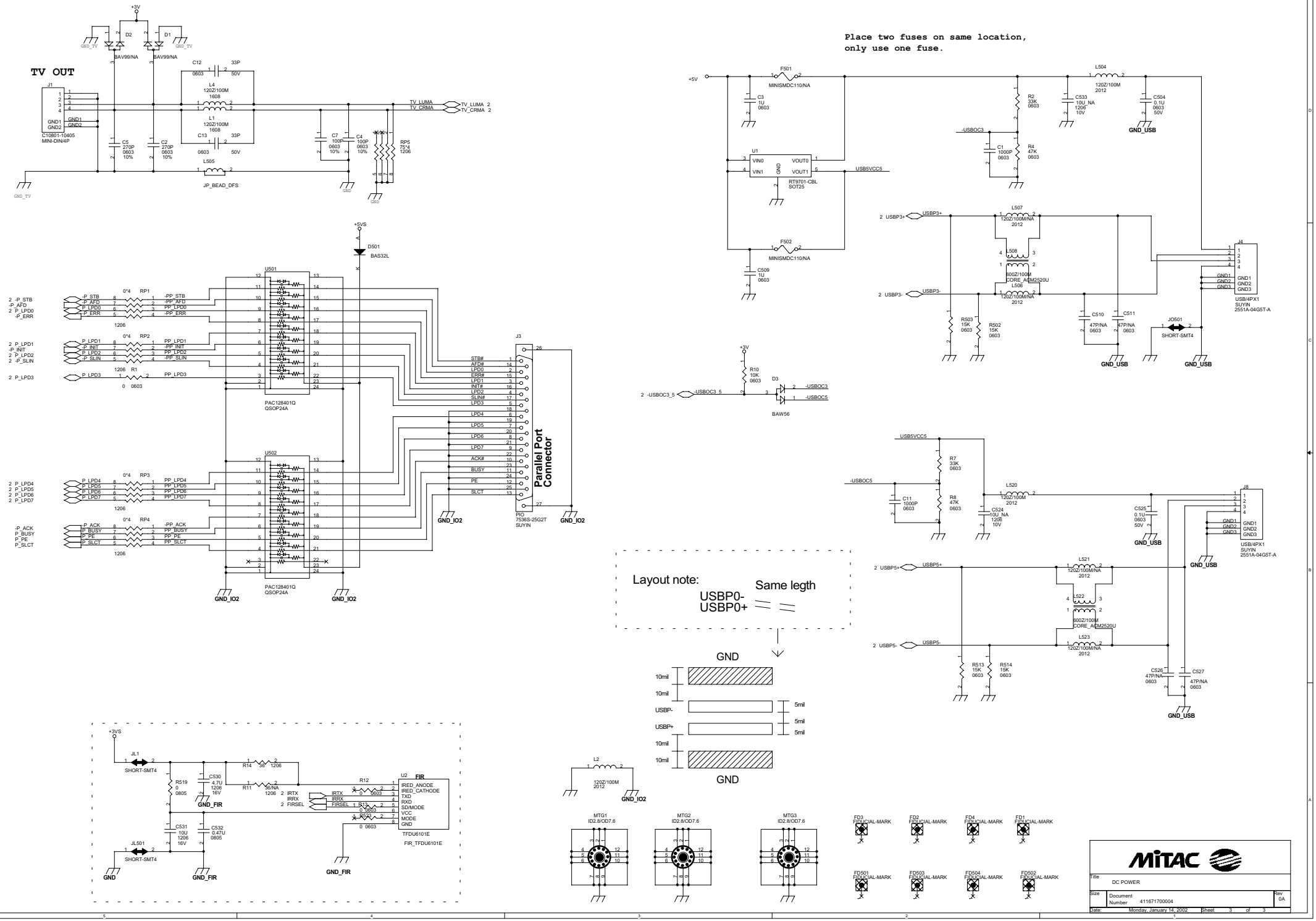
8575/8575N DD BOARD R0A

SYSTEM POWER (+3V +5V +12V)



MiTAC		
Title	SYSTEM POWER	
Size	Document Number 411671700004	Rev 0A
Date: Monday, January 14, 2002	Sheet 1 of 3	


PD504 EC11FS2
PD503 EC11FS2
ALWAYS
PD514 EC31QS04-TE12L DC2010
PD505 EC31QS04-TE12L DC2010
PD506 EC31QS04-TE12L DC2010
PR516 DC2010 4.7K 0805
ADINP
JS501 SHORT-SMT4
JO502 OPEN-SMT4
PU502 SI4835DY SO8
J2 2DC-S107B200
JACK-2P
PF501 TR/SFT-10A FUSE_2917
JO518 JO520 JO519
PL508 120Z/100M 2012
PL501 120Z/100M 2012
PC502 0.1U 0603 50V
PC501 0.1U 0603 50V
PD501 RLZ24D MLL34B
PR506 .02/NA 2512 1%
PR2 0/NA 0603
PR1 0/NA 0603
PR507 470K 0603
PR508 100K 0603
PQ501 2N7002
PR509 1M 0603
PC518 0.1U 0603 50V
PC523 1000P 0603
+DVMAIN
PU1 MAX4173FEUT-T SOT26
+VDD5S
LEARNING
PC4 0.1U 0603 50V
PR3 10 0603
I_LIMIT
PC5 1U 0805 10V
PJ1 HDR/10PX2/H8.49 PH-D-RA-44-X-X CEN
+5V
+3VS
+3V
ADINP
PL1 120Z/100M 2012
PC1 330U 10V
PC6 330U 10V
PC15 0.1U 0603 25V
+5VS
ALWAYS
+D/VMAIN
DVMAIN2
PC520 0.1U 0603 25V +80-20%
PL503 120Z/100M 2012
PL502 120Z/100M 2012
PC519 0.01U 0805
GND
F1 MINISMDC110/NA
C8 1U 0603
U3 RT9701-CBL SOT25
VIN0 VIN1 VOUT0 VOUT1 GND
USB0VCC5
F2 MINISMDC110/NA
C10 1U 0603
L516 120Z/100M 2012
C516 10U_NA 1206 10V
C517 0.1U 0603 50V
GND_USB
R3 33K 0603
C9 1000P 0603
R5 47K 0603
-USBOC1
PQ1 SI2301DS
+12V
+12VS
R7 1M 0603
R9 33 0603
PQ2 2N7002
PSON
R6 1M 0603
PU501 AO4400 SO8
PU503 AO4400 SO8
+5V
+5VS
+3V
+3VS
PR510 470K 0603
PC509 0.1U 0603 50V
PC503 0.1U 0603 50V
R516 10K 0603
D504 BAW56
-USBOC0_1
-USBOC0
-USBOC1
USBP1+
USBP1-
L517 120Z/100M/NA 2012
L518 600Z/100M CORE_ACM2520U
L519 120Z/100M/NA 2012
R508 15K 0603
R509 15K 0603
C520 47P/NA 0603
C521 47P/NA 0603
JO521 SHORT-SMT4
J7 USB/4PX1 SUYIN 2551A-04GST-A
GND1 GND2 GND3
Cover Switch
-LID
R511 1K 0603
SW1 MPU-101-6DB
C522 2.2U 16V 1206
PJ2
MA/22PX2/1.27 SPEED G442-8701-441
-USBOC0 -USBOC3_5 P_BUSY FIRSEL P_PE IRRX IRTX -P_ACK USBP0- USBP0+ USBP1- USBP1+ TV_CRMA TV_LUMA USBP3- USBP3+ +5VAS BLADJ +12VS PSON
-LID I_LIMIT LEARNING P_LPD0 P_LPD1 P_LPD2 P_LPD3 P_LPD4 P_LPD5 P_LPD6 P_LPD7 P_SLCT -P_STB -P_AFD -P_ERR -P_INIT -P_SLIN -AC_POWER -BATT_LED -BATT_G -BATT_R ENPBLT1 PWR_ON USBP5- USBP5+
C514 0.1U_NA 50V 0603
C513 0.1U 0603 50V
ENPBLT1
+5V
BLADJ
L515 L514 L513
BEAD 0603D
BEAD 0805C
BEAD 0603D
FA501
120OHM/100MHZ
-AC_POWER -BATT_LED -BATT_G -BATT_R
J6 Inverter
GND1 GND2
MA/12PX1/ST SPEED Y17-101-0001
+5VAS
L512 BEAD 0805C
C512 0.1U 0603 50V
USB0VCC5
-USBOC0
R506 33K 0603
R518 47K 0603
CS34 1000P 0603
C501 10U_NA 1206 10V
L524 120Z/100M 2012
C506 0.1U 0603 50V
J5 USB/4PX1 SUYIN 2551A-04GST-A
USBP0+
USBP0-
L510 120Z/100M/NA 2012
L509 600Z/100M CORE_ACM2520U
L511 120Z/100M/NA 2012
R504 15K 0603
R505 15K 0603
C505 47P/NA 0603
C507 47P/NA 0603
MiTAC
Title DC POWER
Size
Document Number 411671700004
Rev 0A
Date: Monday, January 14, 2002 Sheet 2 of 3


TV OUT
Place two fuses on same location,
only use one fuse.
Parallel Port Connector
Layout note:
USBP0-
USBP0+
Same legth
PAC128401Q
QSOP24A
PIO
7536S-25G2T
SUYIN
USB/4PX1
SUYIN
2551A-04G5T-A
SHORT-SMT4
BAV99/NA
BAS32L
BAW56
RT9701-CBL
SOT25
MINISMDC110/NA
TFDU6101E
FIR_TFDU6101E
MITAC
DC POWER
Monday, January 14, 2002

Reference Material

❖ Intel Pentium 4 Processor mPGA478 Socket	Intel, INC
❖ SiS650 IGUI Host / Memory Controller	SiS, INC
❖ SiS691 MuTIOL Media I/O Controller	SiS, INC
❖ SiS301LV / Chrontel CH7019 TV/LVDS Encoder	SiS, INC
❖ PCI1410GGU PCMCIA Controller	TI, INC
❖ uPD72872 IEEE1394 Controller	NEC, INC
❖ 8575 Hardware Engineering Specification	*Technology Corp.*/MiTAC

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Author : Sissel Diao

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Tel : 886-3-5779250 Fax : 886-3-5781245

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E-mail : Willy.Chen @ mic.com.tw

Web : http: //www.mitac.com http: //www.mitacservice.com